PRELIMINARY

intel®

SERIES 2 FLASH MEMORY CARDS
iMC004FLSA, iMC010FLSA, iMC020FLSA

- 4, 10 and 20 Megabyte Capacities
- PCMCIA 2.0/JEIDA 4.1 68-Pin Standard
  - — Hardwired Card Information Structure
  - — Byte- or Word-Wide Selectable
- ExCA™ Compatible for System-to-System Inter-Operability
- Component Management Registers for Card Status/Control and Flexible System Interface
- Automatic Erase/Write
  - — Monitored with Ready/Busy Output
- Card Power-Down Modes
  - — Deep-Sleep for Low Power Applications
- Mechanical Write Protect Switch
- Solid-State Reliability
- Intel FlashFile™ Architecture
- High-Performance Read Access
  - — 200 ns Maximum
- High-Performance Random Writes
  - — 10 μs Typical Word Write
- Erase Suspend to Read Command
  - — Keeps Erase as Background Task
- Nonvolatility (Zero Retention Power)
  - — No Batteries Required for Back-up
- ETOX™ III 0.8μ Flash Memory Technology
  - — 5V Read, 12V Erase/Write
  - — High-Volume Manufacturing Experience

Intel's Series 2 Flash Memory Card facilitates high-performance disk emulation in mobile PCs and dedicated equipment. Manufactured with Intel's ETOX III 0.8μ, FlashFile Memory devices, the Series 2 Card allows code and data retention while erasing and/or writing other blocks. Additionally, the Series 2 Flash Memory Card features low power modes, flexible system interfacing and a 200 ns read access time. When coupled with popular low-power microprocessors, like Intel's 386SL™, these cards enable high-performance implementations of mobile computers and systems.

Series 2 Cards conform to the Personal Computer Memory Card International Association (PCMCIA 2.0)/Japanese Electronics Industry Development Association (JEIDA 4.1) 68-pin standard, providing electrical and physical compatibility. The Series 2 Flash Memory Card is also compatible with Intel's Exchangeable Card Architecture (ExCA), an open hardware and software system implementation of PCMCIA Release 2.0 that allows inter-operability from system to system, independent of manufacturer.

Data file management software, such as Microsoft's* Flash File System (FFS), provide data file storage and memory management, much like a disk operating system. Intel's Series 2 Flash Memory Cards, coupled with flash file management software, effectively provide a removable, all-silicon mass storage solution with higher performance and reliability than disk-based memory architectures.

Designing with Intel's FlashFile Architecture enables OEM system manufacturers to design and manufacture a new generation of mobile PCs and dedicated equipment where high performance, ruggedness, long battery life and lighter weight are a requirement. For large user groups in workstation environments, the Series 2 Cards provide a means to securely store user data and backup system configuration/status information.

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Microsoft is a trademark of Microsoft Corporation.

October 1992
Order Number: 290434-002

Table 1. Series 2 Flash Memory Card Pinout

Pin	Signal	I/O	Function	Active	Pin	Signal	I/O	Function	Active
1	GND		Ground		35	GND		Ground	
2	DQ_3	I/O	Data Bit 3		36	$\overline{CD}_1$	O	Card Detect 1	LO
3	DQ_4	I/O	Data Bit 4		37	DQ_{11}	I/O	Data Bit 11	
4	DQ_5	I/O	Data Bit 5		38	DQ_{12}	I/O	Data Bit 12	
5	DQ_6	I/O	Data Bit 6		39	DQ_{13}	I/O	Data Bit 13	
6	DQ_7	I/O	Data Bit 7		40	DQ_{14}	I/O	Data Bit 14	
7	$\overline{CE}_1$	I	Card Enable 1	LO	41	DQ_{15}	I/O	Data Bit 15	
8	A_{10}	I	Address Bit 10		42	$\overline{CE}_2$	I	Card Enable 2	LO
9	$\overline{OE}$	I	Output Enable	LO	43	NC			
10	A_{11}	I	Address Bit 11		44	RFU		Reserved	
11	A_9	I	Address Bit 9		45	RFU		Reserved	
12	A_8	I	Address Bit 8		46	A_{17}	I	Address Bit 17	
13	A_{13}	I	Address Bit 13		47	A_{18}	I	Address Bit 18	
14	A_{14}	I	Address Bit 14		48	A_{19}	I	Address Bit 19	
15	$\overline{WE}$	I	Write Enable	LO	49	A_{20}	I	Address Bit 20	
16	RDY/$\overline{BSY}$	O	Ready-Busy	HI/LO	50	A_{21}	I	Address Bit 21	
17	V_{CC}		Supply Voltage		51	V_{CC}		Supply Voltage	
18	V_{PP1}		Supply Voltage		52	V_{PP2}		Supply Voltage	
19	A_{16}	I	Address Bit 16		53	A_{22}	I	Address Bit 22	
20	A_{15}	I	Address Bit 15		54	A_{23}	I	Address Bit 23	
21	A_{12}	I	Address Bit 12		55	A_{24}	I	Address Bit 24	
22	A_7	I	Address Bit 7		56	A_{25}		No Connect	
23	A_6	I	Address Bit 6		57	RFU		Reserved	
24	A_5	I	Address Bit 5		58	RST	I	Reset	HI
25	A_4	I	Address Bit 4		59	WAIT	O	Extend Bus Cycle	LO
26	A_3	I	Address Bit 3		60	RFU		Reserved	
27	A_2	I	Address Bit 2		61	$\overline{REG}$	I	Register Select	LO
28	A_1	I	Address Bit 1		62	BVD_2	O	Batt. Volt Det 2	
29	A_0	I	Address Bit 0		63	BVD_1	O	Batt. Volt Det 1	
30	DQ_0	I/O	Data Bit 0		64	DQ_8	I/O	Data Bit 8	
31	DQ_1	I/O	Data Bit 1		65	DQ_9	I/O	Data Bit 9	
32	DQ_2	I/O	Data Bit 2		66	DQ_{10}	I/O	Data Bit 10	
33	WP	O	Write Protect	HI	67	$\overline{CD}_2$	O	Card Detect 2	LO
34	GND		Ground		68	GND		Ground	

Table 2. Series 2 Flash Memory Card Pin Descriptions

Symbol	Type	Name and Function
A_0–A_{25}	I	**ADDRESS INPUTS:** A_0 through A_{25} are address bus lines which enable direct addressing of 64 megabytes of memory on a card. A_0 is not used in word access mode. A_{24} is the most significant address bit. Note: A_{25} is a no-connect but should be provided on host side.
DQ_0–DQ_{15}	I/O	**DATA INPUT/OUTPUT:** DQ_0 through DQ_{15} constitute the bidirectional data bus. DQ_{15} is the most significant bit.
$\overline{CE}_1$, $\overline{CE}_2$	I	**CARD ENABLE 1, 2:** $\overline{CE}_1$ enables even bytes, $\overline{CE}_2$ enables odd bytes. Multiplexing A_0, $\overline{CE}_1$ and $\overline{CE}_2$ allows 8-bit hosts to access all data on DQ_0 through DQ7. (See Table 3 for a more detailed description.)
$\overline{OE}$	I	**OUTPUT ENABLE:** Active low signal gating read data from the memory card.
$\overline{WE}$	I	**WRITE ENABLE:** Active low signal gating write data to the memory card.
RDY/$\overline{BSY}$	O	**READY/BUSY OUTPUT:** Indicates status of internally timed erase or write activities. A high output indicates the memory card is ready to accept accesses. A low output indicates that a device(s) in the memory card is(are) busy with internally timed activities. See text for an alternate function (READY-BUSY MODE REGISTER).
$\overline{CD}_1$ & $\overline{CD}_2$	O	**CARD DETECT 1, 2:** These signals provide for correct card insertion detection. They are positioned at opposite ends of the card to detect proper alignment. The signals are connected to ground internally on the memory card and will be forced low whenever a card is placed in the socket. The host socket interface circuitry shall supply 10K or larger pull-up resistors on these signal pins.
WP	O	**WRITE PROTECT:** Write Protect reflects the status of the Write-Protect switch on the memory card. WP set high = write protected, providing internal hardware write lockout to the flash array.
V_{PP1}, V_{PP2}		**WRITE/ERASE POWER SUPPLY:** (12V nominal) for erasing memory array blocks or writing data in the array. They must be 12V to perform an erase/write operation. V_{PP1} supplies even byte Erase/Write voltage and V_{PP2} supplies the odd byte Erase/Write voltage.
V_{CC}		**CARD POWER SUPPLY** (5V nominal) for all internal circuitry.
GND	I	**GROUND** for all internal circuitry.
$\overline{REG}$	I	**REGISTER SELECT** provides access to Series 2 Flash Memory Card registers and Card Information Structure in the Attribute Memory Plane.
RST	I	**RESET** from system, active high. Places card in Power-On Default State. RESET pulse width must be ≥ 200 ns.
$\overline{WAIT}$	O	**WAIT (Extend Bus Cycle)** is used by Intel's I/O cards and is driven high.
BVD_1, BVD_2	O	**BATTERY VOLTAGE DETECT:** Upon completion of the power on reset cycle, these signals are driven high to maintain SRAM-card compatibility.
RFU		**RESERVED FOR FUTURE USE**
NC		**NO INTERNAL CONNECTION.** Pin may be driven or left floating.

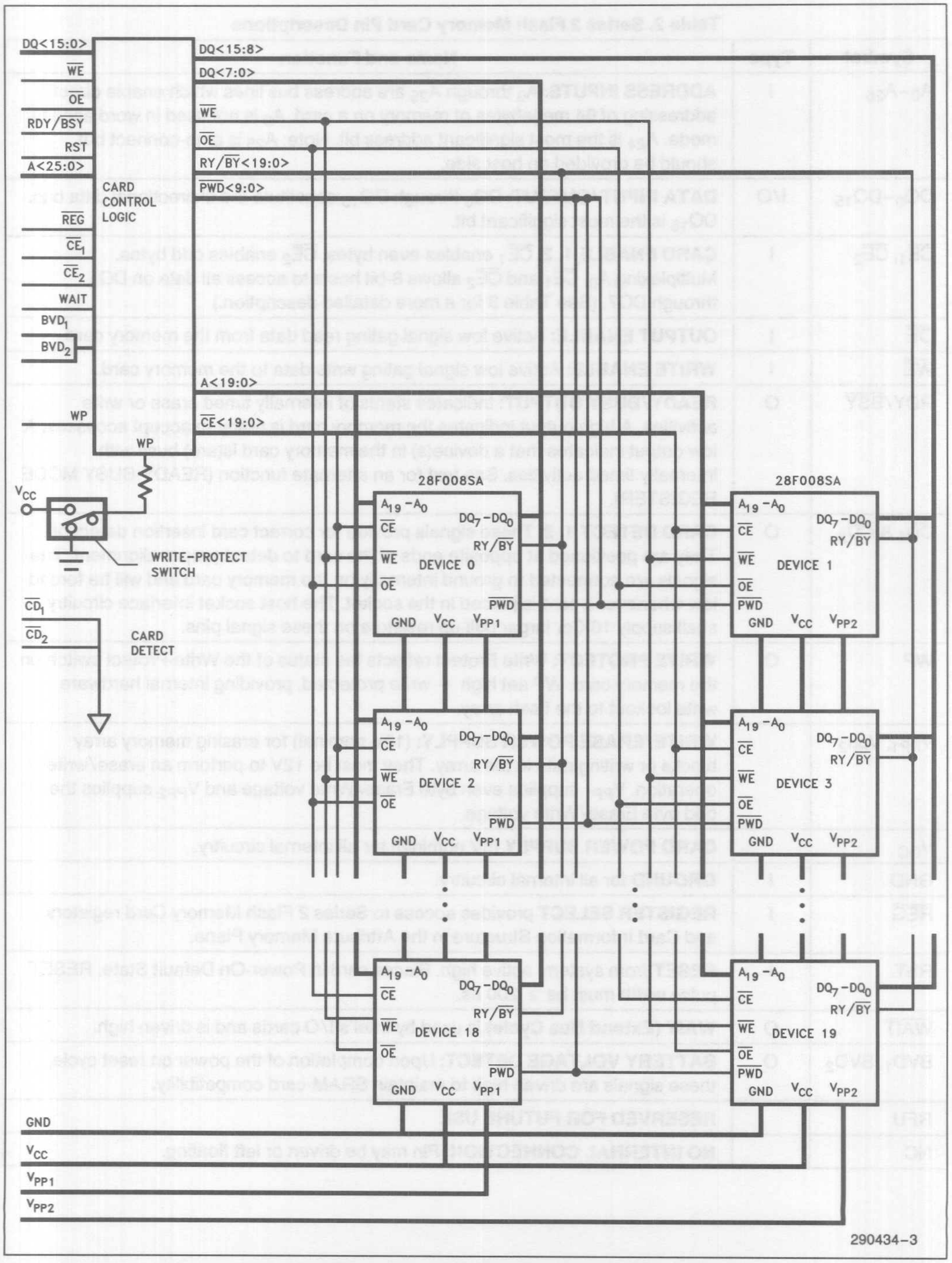


Figure 1. Detailed Block Diagram. The Card Control Logic Provides Decoding Buffering and Control Signals.

APPLICATIONS

Intel's second generation Series 2 Flash Memory Cards facilitate high performance disk emulation for the storage of data files and application programs on a purely solid-state removable medium. File management software, such as Microsoft's Flash File System, in conjunction with the Series 2 Flash Memory Cards enable the design of high-performance light-weight notebook, palmtop, and pen-based PCs that have the processing power of today's desktop computers.

Application software stored on the flash memory card substantially reduces the slow disk-to-DRAM download process. Replacing the mechanical disk results in a dramatic enhancement of read performance and substantial reduction of power consumption, size and weight—considerations particularly important in portable PCs and equipment. The Series 2 Card's high performance read access time allows the use of Series 2 Cards in an "execute-in-place" (XIP) architecture. XIP eliminates redundancy associated with DRAM/Disk memory system architectures. Operating systems stored in Flash Memory decreases system boot or program load times, enabling the design of PCs that boot, operate, store data files and execute application programs from/to nonvolatile memory without losing the ability to perform an update.

File management systems modify and store data files by allocating flash memory space intelligently. Wear leveling algorithms, employed to equally distribute the number of rewrite cycles, ensure that no particular block is cycled excessively relative to other blocks. This provides hundreds of thousands of hours of power on usage.

This file management software enables the user to interact with the flash memory card in precisely the same way as a magnetic disk.

For example, the Microsoft Flash File System enables the storage and modification of data files by utilizing a linked-list directory structure that is evenly distributed along with the data throughout the memory array. The linked-list approach minimizes file fragmentation losses by using variable-sized data structures rather than the standard sector/cluster method of disk-based systems.

Implementation of Intel's Exchangeable Card Architecture (ExCA) enables the user to transport files and application programs between portable and desktop PCs via memory card Reader/Writers. Series 2 Flash Memory Cards provide durable nonvolatile memory storage for mobile PCs on the road, facilitating simple transfer back into the desktop environment.

For systems currently using a static RAM/battery configuration for data acquisition, the Series 2 Flash Memory Card's nonvolatility eliminates the need for battery backup. The concern for battery failure no longer exists, an important consideration for portable computers and medical instruments, both requiring continuous operation. Series 2 Cards consume no power when the system is off, and only 5 μA in Deep-Sleep mode (20 Megabyte card). Furthermore, Flash Memory Cards offer a considerable cost and density advantage over memory cards based on static RAM with battery backup.

Besides disk emulation, the Series 2 Card's electrical block-erasure, data writability, and inherent nonvolatility fit well with data accumulation and recording needs. Electrical block-erasure provides design flexibility to selectively rewrite blocks of data, while saving other blocks for infrequently updated parameters and lookup tables. For example, networks and systems that utilize large banks of battery-backed DRAM to store configuration and status benefit from the Series 2 Flash Card's nonvolatility and reliability.

SERIES 2 ARCHITECTURE OVERVIEW

The Series 2 Flash Memory Card contains a 2 to 20 Megabyte Flash Memory array consisting of 2 to 20 28F008SA FlashFile Memory devices. Each 28F008SA contains sixteen individually-erasable, 64 Kbyte blocks; therefore, the Flash Memory Card contains from 32 to 320 device blocks. It also contains two Card Control Logic devices that manage the external interface, address decoding, and component management logic. (Refer to Figure 1 for a block diagram.)

To support PCMCIA-compatible word-wide access, devices are paired so that each accessible memory block is 64 KWords (see Figure 2). Card logic allows the system to write or read one word at a time, or one byte at a time by referencing the high or low byte. Erasure can be performed on the entire block pair (high and low device blocks simultaneously), or on the high or low byte portion separately.

Also in accordance with PCMCIA specifications this product supports byte-wide operation, in which the flash array is divided into 128K x 8 bit device blocks. In this configuration, odd bytes are multiplexed onto the low byte data bus.

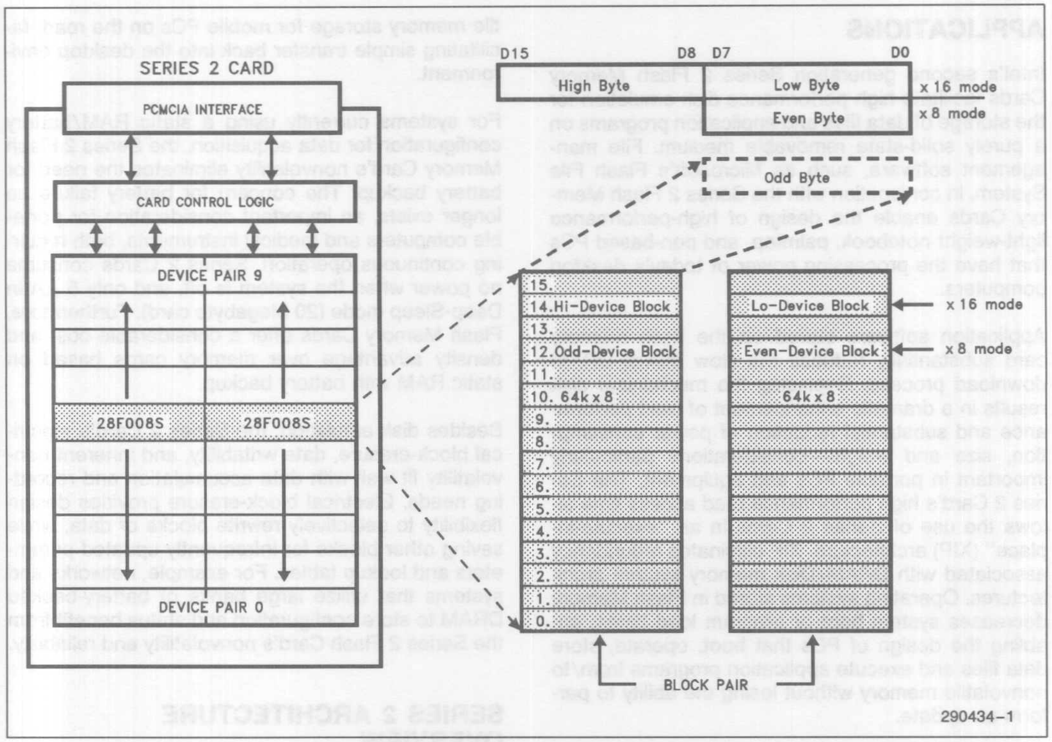


Figure 2. Memory Architecture. Each Device Pair Consists of Sixteen 64 KWord Blocks.

Series 2 Flash Memory Cards offer additional features over the Bulk Erase Flash Card product family (refer to iMC001FLKA, iMC002FLKA and iMC004FLKA data sheets). Some of the more notable enhancements include: high density capability, erase blocking, internal write/erase automation, erase suspension to read, Component Management Registers that provide software control of device-level functions and a deep-sleep mode.

Erase blocking facilitates solid-state storage applications by allowing selective memory reclamation. Multiple 64 Kbyte blocks may be simultaneously erased within the memory card as long as not more than one block per device is erasing. This shortens the total time required for erasure, but requires additional supply current. A block typically requires 1.6 seconds to erase. Each memory block can be erased and completely written 100,000 times.

Erase suspend allows the system to temporarily interrupt a block erase operation. This mode permits reads from alternate device blocks while that same device contains an erasing block. Upon completion of the read operation, erasure of the suspended block must be resumed.

Write/erase automation simplifies the system software interface to the card. A two-step command sequence initiates write or erase operations and provides additional data security. Internal device circuits automatically execute the algorithms and timings necessary for data-write or block-erase operations, including verifications for long-term data integrity. While performing either data-write or block-erase, the memory card interface reflects this by bringing its RDY/$\overline{\text{BSY}}$ (Ready/Busy) pin low. This output goes high when the operation completes. This feature reduces CPU overhead and allows software polling or hardware interrupt mechanisms. Writing memory data is achieved in single byte or word increments, typically in 10 μs.

Read access time is 200 ns or less over the 0°C to 60°C temperature range.

The deep-sleep mode reduces power consumption to 5 μA to help extend battery life of portable host systems. Activated through software control, this mode optionally affects the entire flash array (Global PowerDown Register) or specific device pairs (Sleep Control Register).

PCMCIA/JEIDA INTERFACE

The Series 2 Flash Memory Card interface supports the PCMCIA 2.0 and JEIDA 4.1 68-pin card format (see Tables 1 and 2). Detailed specifications are described in the PC Card Standard, Release 2.0, September 1991, published by PCMCIA. The Series 2 Card conforms to the requirements of both Release 1 and Release 2 of the PC Card Standard.

Series 2 Card pin definitions are equivalent to the Bulk-Erase Flash Card except that certain No Connects are now used. A_{22} through A_{24}, RST (Reset), and RDY/$\overline{BSY}$ (Ready/Busy) have pin assignments as set by the PCMCIA standard.

NOTE: The READY/BUSY signal is abbreviated as RDY/$\overline{BSY}$ by PCMCIA (card level) and as RY/$\overline{BY}$ by JEDEC (component level).

The outer shell of the Series 2 card meets all PCMCIA/JEIDA Type 1 mechanical specifications. See Figure 19 for mechanical dimensions.

WRITE PROTECT

A mechanical write protect switch provides the card's memory array with internal write lockout. The Write-Protect (WP) output pin reflects the status of this mechanical switch. It outputs a high signal (V_{OH}) when writes are disabled. This switch does not lock out writes to the Component Management Registers.

BATTERY VOLTAGE DETECT

PCMCIA requires two signals, BVD_1 and BVD_2, be supplied at the interface to reflect card battery condition. Flash Memory Cards do not require batteries. When the power on reset cycle is complete, BVD_1 and BVD_2 are driven high to maintain compatibility.

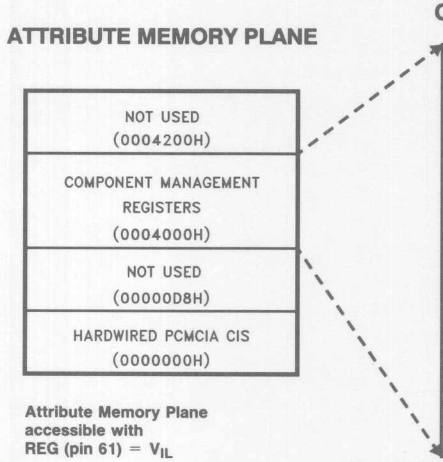
CARD DETECT

Two signals, $\overline{CD}_1$ and $\overline{CD}_2$, allow the host to determine proper socket seating. They reside at opposite ends of the connector and are tied to ground within the memory card.

DESIGN CONSIDERATIONS

The Series 2 Card consists of two separate memory planes: the Common Memory Plane (or Main Memory) and the Attribute Memory Plane. The Common Memory Plane resides in the banks of device pairs and represents the user-alterable memory space.

The Component Management Registers (CMR) and the hardwired Card Information Structure (CIS) reside in the Attribute Memory Plane within the Card Control Logic, as shown in Figure 3. The Card Control Logic interfaces the PCMCIA connector and the internal flash memory array and performs address decoding and data control.



COMPONENT MANAGEMENT REGISTERS

CIS ADDRESS	FUNCTION
4142H - 41FEH	RESERVED
4140H	READY-BUSY MODE (INTEL)
4136H - 413EH	RESERVED
4130H - 4134H	READY-BUSY STATUS (INTEL)
4126H - 412EH	RESERVED
4120H - 4124H	READY-BUSY MASK (INTEL)
411CH - 411EH	RESERVED
4118H - 411AH	SLEEP CONTROL (INTEL)
4106H - 4116H	RESERVED
4104H	WRITE PROTECTION (INTEL)
4102H	RESERVED
4100H	CARD STATUS (INTEL)
4004H - 40FEH	RESERVED
4002H	GLOBAL POWERDOWN (PCMCIA)
4000H	SOFT RESET (PCMCIA)

290434-2

INTEL = **Performance Enhancement Register**
PCMCIA = **Defined in PCMCIA Release 2.0**

Figure 3. Component Management Registers Allow S/W Control of Components within Card

ADDRESS DECODE

Address decoding provides the decoding logic for the 2 to 20 Device Chip Enables and the elements of the Attribute Memory Plane. $\overline{REG}$ selects between the Common Memory Plane ($\overline{REG} = V_{IH}$) and the Attribute Memory Plane ($\overline{REG} = V_{IL}$).

NOTE:

The Series 2 Card has *active* address inputs A_0 to A_{24} implying that reading and writing to addresses beyond 32 Megabytes causes wraparound. Furthermore, reads to illegal addresses (for example, between 20 and 32 Meg on a 20 Megabyte card) returns 0FFFFh data.

The 28F008SA devices, storing data, applications or firmware, form the Common Memory Plane accessed individually or as device pairs. Memory is linearly mapped in the Common Memory Plane. Three memory access modes are available when accessing the Common Memory Plane: Byte-Wide, Word Wide, and Odd-Byte modes.

Additional decoding selects the hardwired PCMCIA CIS and Component Management Registers mapped in the Attribute Memory Plane beginning at address 000000H.

The 512 memory-mapped even-byte CMRs are linearly mapped beginning at address 4000H in the Attribute Memory Plane.

DATA CONTROL

Data Control Logic selects the path and direction for accessing the Common or Attribute Memory Plane. It controls any of the PCMCIA-defined Word-Wide, Byte-Wide or Odd-Byte modes for either reads or writes to these areas. As shown in Table 3, input pins which determine these selections are $\overline{REG}$, A_0 through A_{24}, $\overline{WE}$, $\overline{OE}$, $\overline{CE}_1$, and $\overline{CE}_2$. PCMCIA specifications allow only even-byte access to the Attribute Memory Plane.

In Byte-Wide mode, bytes contiguous in software actually alternate between two device blocks of a device pair. Therefore, erasure of one device block erases every other contiguous byte. In accordance with the PCMCIA standard for memory configuration, the Series 2 Card does not support confining contiguous bytes within one flash device when in by-8 mode.

Table 3. Data Access Mode Truth Table

Function Mode	$\overline{REG}$	$\overline{CE_2}$	$\overline{CE_1}$	A_0	$\overline{OE}$	$\overline{WE}$	V_{PP2}	V_{PP1}	D_{15}–D_8	D_7–D_0
COMMON MEMORY PLANE										
STANDBY[1]	X	H	H	X	X	X	V_{PPL}[2]	V_{PPL}[2]	HIGH-Z	HIGH-Z
BYTE READ	H	H	L	L	L	H	V_{PPL}[2]	V_{PPL}[2]	HIGH-Z	EVEN-BYTE
	H	H	L	H	L	H	V_{PPL}[2]	V_{PPL}[2]	HIGH-Z	ODD-BYTE
WORD READ	H	L	L	X	L	H	V_{PPL}[2]	V_{PPL}[2]	ODD-BYTE	EVEN-BYTE
ODD-BYTE READ	H	L	H	X	L	H	V_{PPL}[2]	V_{PPL}[2]	ODD-BYTE	HIGH-Z
BYTE WRITE	H	H	L	L	H	L	V_{PPH}	V_{PPH}	X	EVEN-BYTE
	H	H	L	H	H	L	V_{PPH}	V_{PPH}	X	ODD-BYTE
WORD WRITE	H	L	L	X	H	L	V_{PPH}	V_{PPH}	ODD-BYTE	EVEN-BYTE
ODD-BYTE WRITE	H	L	H	X	H	L	V_{PPH}	V_{PPL}[2]	ODD-BYTE	X
ATTRIBUTE MEMORY PLANE										
BYTE READ	L	H	L	L	L	H	X[2]	X[2]	HIGH-Z	EVEN-BYTE
	L	H	L	H	L	H	X[2]	X[2]	HIGH-Z	INVALID
WORD READ	L	L	L	X	L	H	X[2]	X[2]	INVALID DATA[3]	EVEN-BYTE
ODD-BYTE READ	L	L	H	X	L	H	X[2]	X[2]	INVALID DATA[3]	HIGH-Z
BYTE WRITE	L	H	L	L	H	L	X[2]	X[2]	X	EVEN-BYTE
	L	H	L	H	H	L	X[2]	X[2]	X	INVALID OPERATION[3]
WORD WRITE	L	L	L	X	H	L	X[2]	X[2]	INVALID OPERATION[3]	EVEN-BYTE
ODD-BYTE WRITE	L	L	H	X	H	L	X[2]	X[2]	INVALID OPERATION[3]	X

NOTES:
1. Standby mode is valid in Common Memory or Attribute Memory access.
2. To meet the low power specifications, $V_{PP} = V_{PPL}$; however V_{PPH} presents no reliability problems.
3. Odd-Byte data are not valid during access to the Attribute Memory Plane.
4. $H = V_{IH}$, $L = V_{IL}$, X = Don't Care.

PRINCIPLES OF OPERATION

Intel's Series 2 Flash Memory Card provides electrically-alterable, non-volatile, random-access storage. Individual 28F008SA devices utilize a Command User Interface (CUI) and Write State Machine (WSM) to simplify block-erasure and data write operations.

COMMON MEMORY ARRAY

Figure 4 shows the Common Memory Plane's organization. The first block pair (64 KWords) of Common Memory, referred to as the Common Memory Card Information Structure Block, *optionally* extends the hardwired CIS in the Attribute Memory Plane for additional card information. This may be written during initial card formatting for OEM customization. Since this CIS Block is part of Common Memory, its data can be altered. Write access to the Common Memory CIS Block is controlled by the Write Protect Control Register which may be activated by system software after power-up. Additionally, the entire Common Memory plane (minus the Common Memory CIS Block) may be software write protected. *Note that the Common Memory CIS Block is not part of the Attribute Memory Plane. Do not assert $\overline{REG}$ to access the Common Memory CIS Block.*

13FFFFFH 1200000H	Device Pair 9
1000000H	Device Pair 8
0E00000H	Device Pair 7
0C00000H	Device Pair 6
0A00000H	Device Pair 5
0800000H	Device Pair 4
0600000H	Device Pair 3
0400000H	Device Pair 2
0200000H	Device Pair 1
0020000H	Device Pair 0
0000000H	Optional CIS

Figure 4. Common Memory Plane. Use the Optional Common Memory Plane CIS for Custom Card Format Information.

HARDWIRED CIS

The card's structure description resides in the even-byte locations starting at 0000H and going to the CIS ending tuple (FNULL) within the Attribute Memory Plane. Data included in the hardwired CIS consists of tuples. Tuples are a variable-length list of data blocks describing details such as manufacturer's name, the size of each memory device and the number of flash devices within the card.

COMPONENT MANAGEMENT REGISTERS (CMRs)

The CMRs in the Attribute Memory Plane provide special, software-controlled functionality. Card Control Logic includes circuitry to access the CMRs. $\overline{REG}$ (PCMCIA, pin 61) selects the Attribute Memory Plane (and therefore the CMRs) when equal to V_{IL}.

CMRs are classified into two categories: those defined by PCMCIA R2.0 and those included by Intel (referred to as Performance Enhancement Registers) to enhance the interface between the host system and the card's flash memory array. CMRs (See Figure 3) provide seven control functions—Ready-Busy Interrupt Mode, Device Ready-Busy Status, Device Ready-Busy Mask, Deep-Sleep Control, Software-controlled Write Protection, Card Status and Soft Reset.

SOFT RESET REGISTER (PCMCIA)

(CONFIGURATION OPTION)

The SOFT RESET REGISTER (Attribute Memory Plane Address 4000H, Figure 5) is defined in the PCMCIA Release 2.0 specification as the Configuration Option Register.

Bit 7 is the soft reset bit (SRESET). Writing a 1 to this bit initiates card reset to the power-on default state (see Side Bar page 11). This bit must be cleared to use the CMRs or to access the devices.

SRESET implements in software what the reset pin implements in hardware. On power-up, the card automatically assumes default conditions. Similar to the reset pin (pin 58), this bit clears at the end of a power-on reset cycle or a system reset cycle.

Bits 0 through 6 are not used by this memory card, but power up as zeroes for PCMCIA compatibility.

SOFT RESET REGISTER

(CONFIGURATION OPTION REGISTER)

(Read/Write Register)

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 4	BIT 2	BIT 1	BIT 0
4000H	SRESET	PCMCIA CONFIGURATION INDEX RESETS TO ZERO ON POWER UP						

1 = RESET, CLEAR TO ACCESS CARD

Figure 5. SOFT RESET REGISTER (PCMCIA). Sets the Memory Card in the Power-On Default State.

POWER-ON DEFAULT CONDITIONS

- All Devices Powered Up In Standby Mode
- Common Memory Available For Writes
- All Device Ready/Busy Outputs Unmasked
- PCMCIA Ready/Busy Mode Enabled
- Ready/Busy Output Goes To Ready

Global PowerDown Register (PCMCIA)

(Configuration and Status)

The Global PowerDown Register (Attribute Memory Plane Address 4002H, Figure 6) is referred to as the Configuration and Status Register in the PCMCIA Release 2.0 specification.

Bit 2 (PwrDwn) controls global card power-down. Writing a 1 to this bit places each device within the card into "Deep-Sleep" mode. *Devices in Deep-Sleep are not accessible.* Recovery from power-down requires 500 ns for reads and 1 μs for writes.

The PWRDWN bit defaults to 0 on card power-up or reset. Setting or clearing this bit has no affect on the bit settings of the Sleep Control Register.

The remaining Global PowerDown Register bits are defined for Intel's family of I/O cards and are driven low for compatibility.

GLOBAL POWER-DOWN REGISTER

(CONFIGURATION AND STATUS REGISTER)

(Read/Write Register)

1 = POWER DOWN

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
4002H	ZEROES					PWRDWN	ZEROES	

Figure 6. GLOBAL POWER-DOWN REGISTER (PCMCIA). The PWRDWN Bit Enables Power-Down of All Flash Memory Devices.

CARD STATUS REGISTER

(Read Only Register)

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
4100H	ADM	ADS	SRESET	CMWP	PWRDWN	CISWP	WP	RDY/$\overline{\text{BSY}}$

Figure 7. CARD STATUS REGISTER (Intel) Provides a Quick Review of the Card's Status

CARD STATUS REGISTER (INTEL)

The Read-Only, CARD STATUS REGISTER (Attribute Memory Plane Address 4100H, Figure 7) returns generalized status of the Series 2 Card and its CMRs.

Bit 0 (RDY/$\overline{\text{BSY}}$) reflects the card's RDY/$\overline{\text{BSY}}$ (Ready-Busy) output. Software polling of this bit provides data-write or block-erase operation status. A zero indicates a busy device(s) in the card.

Bit 1 (WP) reports the position of the card's Write Protection switch with 1 indicating write protected. It reports the status of the WP pin.

Bit 2 (CISWP) reflects whether the Common Memory CIS is write protected using the WRITE PROTECT REGISTER, with 1 indicating write protected.

Bit 3 (PWRDWN) reports whether the entire flash memory array is in "Deep-Sleep" (PowerDown) mode, with 1 indicating "Deep-Sleep". This bit reflects the PWRDWN bit of the GLOBAL POWER-DOWN REGISTER. Powering down *all* device pairs individually (using the Sleep Control Register), also sets this bit.

Bit 4 (CMWP) reports whether the Common Memory Plane (minus Common Memory CIS) is write protected via the WRITE PROTECT REGISTER with 1 indicating write protected.

Bit 5 (SRESET) reflects the SRESET bit of the SOFT RESET REGISTER. It reports that the card is in Soft Reset with 1 indicating reset. When this bit is zero, the flash memory array and CMRs may be accessed, otherwise clear it via the SRESET REGISTER.

Bit 6 (ADS, ANY DEVICE SLEEP) is the "ORed" value of the SLEEP CONTROL REGISTER. Powering down any device pair sets this bit.

Bit 7 (ADM, ANY DEVICE MASKED) is the "ORed" value of the READY/BUSY MASK REGISTER. Masking any device sets this bit.

WRITE PROTECTION REGISTER (INTEL)

The WRITE PROTECTION REGISTER (Attribute Memory Plane Address 4104H, Figure 8) selects whether the optional Common Memory CIS and the remaining Common Memory blocks are write protected (see Figure 4).

Enable Common Memory CIS write protection by writing a 1 to the CISWP Bit (bit 0).

Enable write protection of the remaining Common Memory blocks by writing a 1 to the CMWP Bit (bit 1).

In the power-on default state, both bits are 0, and therefore not write protected.

Reserved bits (2–7) have undefined values and should be written as zeroes for future compatibility.

WRITE PROTECTION REGISTER

(Read/Write Register)

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
4104H	RESERVED FOR FUTURE USE						CMWP	CISWP

1 = WRITE PROTECT

Figure 8. WRITE PROTECTION REGISTER (Intel) Eliminates Accidental Data Corruption

SLEEP CONTROL REGISTER (INTEL)

Unlike the GLOBAL POWERDOWN REGISTER, which simultaneously places all flash memory devices into a Deep-Sleep mode, the SLEEP CONTROL REGISTER (Attribute Memory Plane Address 4118H–411AH, Figure 9) allows selective power-down control of individual device pairs.

Writing a 1 to a specific bit of the SLEEP CONTROL REGISTER places the corresponding device pair into the "Deep-Sleep" mode. *Devices in Deep-Sleep are not accessible*. On cards with fewer than 20 Megabytes (10 device pairs), writing a one to an absent device pair has no affect and reads back as zero.

This register contains all zeroes (i.e., not in Deep-Sleep mode) when the card powers up or after a hard or soft reset. Furthermore, the Global Power-Down Register has no affect on the contents of this register. Therefore, any bit settings of the Sleep Control Register will remain unchanged after returning from a global power down (writing a zero to the PWRDWN bit of the Global PowerDown Register).

READY-BUSY STATUS REGISTER (INTEL)

The bits in the Read-only, READY-BUSY Status Register (Attribute Memory Plane Address 4130H-4134H, Figure 10) reflect the status (READY = 1, BUSY = 0) of each device's RY/$\overline{\text{BY}}$ output. A busy condition indicates that a device is currently processing a data-write or block-erase operation.

These bits are logically "AND-ed" to form the Ready/Busy output (RDY/$\overline{\text{BSY}}$, pin 16) of the PCMCIA interface. On memory cards with fewer than 20 devices, unused Device RY/$\overline{\text{BY}}$ Status Register bits appear as ready.

SLEEP CONTROL REGISTER

(Read/Write Register)

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
411AH	RESERVED						DEVICES 18/19	DEVICES 16/17
4118H	DEVICES 14/15	DEVICES 12/13	DEVICES 10/11	DEVICES 8/9	DEVICES 6/7	DEVICES 4/5	DEVICES 2/3	DEVICES 0/1

1 = SELECTED DEVICE PAIR IN POWER-DOWN MODE

Figure 9. SLEEP CONTROL REGISTER (Intel) Allows Specific Devices to be Put into Power-Down Mode

READY-BUSY STATUS REGISTER

(Read/Write Register)

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
4134H	RESERVED				DEVICE 19	DEVICE 18	DEVICE 17	DEVICE 16
4132H	DEVICE 15	DEVICE 14	DEVICE 13	DEVICE 12	DEVICE 11	DEVICE 10	DEVICE 9	DEVICE 8
4130H	DEVICE 7	DEVICE 6	DEVICE 5	DEVICE 4	DEVICE 3	DEVICE 2	DEVICE 1	DEVICE 0

1 = DEVICE READY, 0 = DEVICE BUSY

Figure 10. READY-BUSY STATUS REGISTER (Intel) Provides Operation Status of All Flash Memory Devices

READY-BUSY MASK REGISTER (INTEL)

The bits of the Read/Write READY-BUSY MASK REGISTER (Attribute Memory Plane Address 4120H–4124H, Figure 11) mask out the corresponding "AND-ed" READY-BUSY STATUS REGISTER bits from the PCMCIA data bus (RDY/$\overline{\text{BSY}}$, pin 16) and the CARD STATUS REGISTER RDY/$\overline{\text{BSY}}$ Bit (bit 0).

In an unmasked condition (MASK REGISTER bits = 0), any device RY/$\overline{\text{BY}}$ output going low pulls the card's RDY/$\overline{\text{BSY}}$ output to V_{IL} (BUSY). In this case, all devices must be READY to allow the card's RDY/$\overline{\text{BSY}}$ output to be ready (V_{IH}). *This is referred to as the PCMCIA READY-BUSY MODE. An alternate type of READY-BUSY function is described in the next section, READY-BUSY MODE REGISTER.*

READY-BUSY MASK

(Read/Write Register)

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
4124H	RESERVED				DEVICE 19	DEVICE 18	DEVICE 17	DEVICE 16
4122H	DEVICE 15	DEVICE 14	DEVICE 13	DEVICE 12	DEVICE 11	DEVICE 10	DEVICE 9	DEVICE 8
4120H	DEVICE 7	DEVICE 6	DEVICE 5	DEVICE 4	DEVICE 3	DEVICE 2	DEVICE 1	DEVICE 0

1 = MASK ENABLED

Figure 11. READY-BUSY MASK REGISTER (Intel) Essential for Write Optimization

If the READY-BUSY MASK REGISTER bits are set to ones (masked condition), the RDY/$\overline{\text{BSY}}$ output and the CARD STATUS REGISTER RDY/$\overline{\text{BSY}}$ bit will reflect a READY condition regardless of the state of the corresponding devices. The READY-BUSY MASK REGISTER does not affect the READY-BUSY STATUS REGISTER allowing software polling to determine operation status.

Unmasked is the default condition for the bits in this register. On memory cards with fewer than 20 devices, unused device mask bits appear as masked.

READY-BUSY MODE REGISTER (INTEL)

The READY-BUSY MODE REGISTER (Attribute Memory Plane Address 4140H, Figure 12) provides the selection of two types of system interfacing for the busy-to-ready transition of the card's RDY/$\overline{\text{BSY}}$ pin:

1. The standard PCMCIA READY-BUSY MODE, in which the card's RDY/$\overline{\text{BSY}}$ signal generates a low-to-high transition (from busy to ready) only after *all* busy devices (not including masked devices) have completed their data-write or block-erase operations. This may result in a long interrupt latency.
2. A High-Performance mode that generates a low-to-high (from busy-to-ready) transition after each device becomes ready. This provides the host system with immediate notification that a specific device's operation has completed and that device may now be used. This is particularly useful in a file management application where a block pair, containing only deleted files, is being erased to free up space so new file data may be written.

Enabling the HIGH-PERFORMANCE READY-BUSY MODE requires a three step sequence:

1. Set all bits in the READY/BUSY MASK REGISTER. This prevents ready devices from triggering an unwanted interrupt when step 3 is performed.
2. Write 01H to the READY-BUSY MODE REGISTER. This sets the MODE bit.
3. Write 01H to the READY-BUSY MODE REGISTER. This clears the RACK bit.

The MODE and RACK bits *must* be written in the prescribed sequence, *not* simultaneously. The card's circuitry is designed purposely in this manner to prevent an initial, unwanted busy-to-ready transition. Note that in Step 2, writing to the RACK bit is a Don't Care.

When the High-Performance Mode is enabled, specific READY-BUSY MASK bits must be cleared after an operation is initiated on the respective devices. After each device becomes ready, the RDY/$\overline{\text{BSY}}$ pin makes a low-to-high transition. To catch the next device's completion of an operation, the RACK bit must be cleared.

READY-BUSY MODE REGISTER

(Read/Write Register)

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
4140H	RESERVED FOR FUTURE USE						RACK	MODE

MODE = READY-BUSY MODE
0 = PCMCIA MODE
1 = HIGH PERFORMANCE

RACK = READY ACKNOWLEDGE CLEAR TO SET UP RDY/$\overline{\text{BSY}}$ PIN, THEN CLEAR AFTER EACH DEVICE BECOMES READY TO ACKNOWLEDGE TRANSITION.

Figure 12. High Performance Ready-Busy Mode REGISTER (Intel) Used to Trigger a Ready Interrupt for Each Device

PRINCIPLES OF DEVICE OPERATION

Individual 28F008SA devices include a Command User Interface (CUI) and a Write State Machine (WSM) to manage write and erase functions in each device block.

The CUI serves as the device's interface to the Card Control Logic by directing commands to the appropriate device circuitry (Table 4). It allows for fixed power supplies during block erasure and data writes. The CUI handles the $\overline{WE}$ interface into the device data and address latches, as well as system software requests for status while the WSM is operating.

The CUI itself does not occupy an addressable memory location. The CUI provides a latch used to store the command and address and data information needed to execute the command. Erase Setup and Erase Confirm commands require both appropriate command data and an address within the block to be erased. The Data Write Setup command requires both appropriate command data and the address of the location to be written, while the Data Write command consists of the data to be written and the address of the location to be written.

The CUI initiates flash memory writing and erasing operations only when V_{PP} is at 12V. Depending on the application, the system designer may choose to make the V_{PP} power supply switchable (available when writes and erases are required) or hardwired to V_{PPH}. When $V_{PP} = V_{PPL}$, power savings are incurred and memory contents cannot be altered. The CUI architecture provides protection from unwanted write and erase operations even when high voltage is applied to V_{PP}. Additionally, all functions are disabled whenever V_{CC} is below the write lockout voltage V_{LKO}, or when the card's Deep-Sleep modes are enabled. The WSM automates the writing and erasure of blocks within a device. This on-chip state machine controls block erase and data-write, freeing the host processor for other tasks. After receiving the Erase Setup and Erase Confirm commands from the CUI, the WSM controls block-erase. Progress is monitored via the device's status register, the card's control logic, and the RDY/$\overline{BSY}$ pin of the PCMCIA interface. Data-write is similarly controlled, after destination address and expected data are supplied.

Table 4. Device Command Set

28F008SA Command(1)	Bus Cycles Req'd	First Bus Cycle				Second Bus Cycle			
		Operation	Addr(2)	Data x8 Mode	Data x16 Mode	Operation	Addr(2)	Data x8 Mode	Data x16 Mode
Read Array/Reset	1	Write	DA	FFH	FFFFH				
intelligent Identifer	3	Write	DA	90H	9090H	Read	IA	IID(3)	IID(3)
Read Device Status Register	2	Write	DA	70H	7070H	Read	DA	SRD(4)	SRD(4)
Clear Device Status Register	1	Write	DA	50H	5050H				
Erase Setup/Erase Confirm	2	Write	BA	20H	2020H	Write	BA	D0H	D0D0H
Erase Suspend/ Erase Resume	2	Write	DA	B0H	B0B0H	Write	DA	D0H	D0D0H
Write Setup/Write	2	Write	WA	40H	4040H	Write	WA	WD(5)	WD(5)
Alternate Write Setup/Write(6)	2	Write	WA	10H	1010H	Write	WA	WD(5)	WD(5)

NOTES:
1. Commands other than those shown above are reserved by Intel for future device implementations and should not be used.
2. DA = A device-level (or device pair) address within the card.
   BA = Address within the block of a specific device (device pair) being erased.
   WA = Address of memory location to be written.
   IA = A device-level address; 00H for manufacturer code, 01 for device code.
3. Following the intelligent identifier command, two read operations access manufacturer (89H) and device codes (A2H).
4. SRD = Data read from Device Status Register.
5. WD = Data to be written at location WA. Data is latched on the rising edge of $\overline{WE}$.
6. Either 40H or 10H are recognized by the WSM as the Write Setup command.

COMMAND DEFINITIONS

Read Array (FFH) —

Upon initial card power-up, after exit from the Deep-Sleep modes, and whenever illegal commands are given, individual devices default to the Read Array mode. This mode is also entered by writing FFH into the CUI. In this mode, microprocessor read cycles retrieve array data. Devices remain enabled for reads until the CUI receives an alternate command. Once the internal WSM has started a block-erase or data-write operation within a device, that device will not recognize the Read Array command until the WSM has completed its operation (or the Erase Suspend command is issued during erase).

Intelligent Identifier (90H) —

After executing this command, the intelligent identifier values can be read. Only address A_0 of each device is used in this mode, all other address inputs are ignored [(Manufacturer code = 89H for A_0 = 0), (Device code = A2H for A_0 = 1)]. The device will remain in this mode until the CUI receives another command.

This information is useful by system software in determining what type of flash memory device is contained within the card and allows the correct matching of device to write and erase algorithms. System software that fully utilizes the PCMCIA specification will not use the intelligent identifier mode, as this data is available within the Card Information Structure (refer to section on PCMCIA Card Information Structure).

Read Status Register (70H)

After writing this command, a device read outputs the contents of its Status Register, regardless of the address presented to that device. The contents of this register are latched on the falling edge of $\overline{OE}$, $\overline{CE}_1$ (and/or $\overline{CE}_2$), whichever occurs last in the read cycle. This prevents possible bus errors which might occur if the contents of the Status Register changed while reading its contents. $\overline{CE}_1$ (and $\overline{CE}_2$ for odd-byte or word access) or $\overline{OE}$ must be toggled with each subsequent status read, or the completion of a write or erase operation will not be evident. This command is executable while the WSM is operating, however, during a block-erase or data-write operation, reads from the device will automatically return status register data. Upon completion of that operation, the device remains in the Status Register read mode until the CUI receives another command.

The read Status Register command functions when $V_{PP} = V_{PPL}$ or V_{PPH}.

Clear Status Register (50H)

The Erase Status and Write Status bits may be set to "1"s by the WSM and can only be reset by the Clear Status Register Command. These bits indicate various failure conditions. By allowing system software to control the resetting of these bits, several operations may be performed (such as cumulatively writing several bytes or erasing multiple blocks in sequence). The device's Status Register may then be polled to determine if an error occurred during that sequence. This adds flexibility to the way the device may be used.

Additionally, the V_{PP} Status bit (SR.3) MUST be reset by system software (Clear Status Register command) before further block-erases are attempted (after an error).

The Clear Status Register command functions when $V_{PP} = V_{PPL}$ or V_{PPH}. This command puts the device in the Read Array mode.

Write Setup/Write

A two-command sequence executes a data-write operation. After the system switches V_{PP} to V_{PPH}, the write setup command (40H) is written to the CUI of the appropriate device, followed by a second write specifying the address and write data (latched on the rising edge of $\overline{WE}$). The device's WSM controls the data-write and write verify algorithms internally. After receiving the two-command write sequence, the device automatically outputs Status Register data when read (see Figure 13). The CPU detects the completion of the write operation by analyzing card-level or device-level indicators. Card-level indicators include the RDY/$\overline{BSY}$ pin and the READY-BUSY STATUS REGISTER; while device-level indicators include the specific device's Status Register. Only the Read Status Register command is valid while the write operation is active. Upon completion of the data-write sequence (see section on Status Register) the device's Status Register reflects the result of the write operation. The device remains in the Read Status Register mode until the CUI receives an alternate command.

Erase Setup/Erase Confirm Commands (20H)

Within a device, a two-command sequence initiates an erase operation on one device block at a time. After the system switches V_{PP} to V_{PPH}, an Erase Setup command (20H) prepares the CUI for the Erase Confirm command (D0H). The device's WSM controls the erase algorithms internally. After receiving the two-command erase sequence, the device automatically outputs Status Register data when read (see Figure 14). If the command after erase setup is not an Erase Confirm command, the CR sets the Write Failure and Erase Failure bits of the Status Register, places the device into the Read Status Register mode, and waits for another command. The Erase Confirm command enables the WSM for erase (simultaneously closing the address latches for that device's block (A_{16}–A_{19}). The CPU detects the completion of the erase operation by analyzing card-level or device-level indicators. Card-level indicators include the RDY/BSY pin and the READY-BUSY STATUS REGISTER; while device-level indicators include the specific device's Status Register. Only the Read Status Register and Erase Suspend command is valid during an active erase operation. Upon completion of the erase sequence (see section on Status Register) the device's Status Register reflects the result of the erase operation. The device remains in the Read Status Register mode until the CUI receives an alternate command.

The two-step block-erase sequence ensures that memory contents are not accidentally erased. Erase attempts while $V_{PPL} < V_{PP} < V_{PPH}$ produce spurious results and are not recommended. Reliable block erasure only occurs when $V_{PP} = V_{PPH}$. In the absence of this voltage, memory contents are protected against erasure. If block erase is attempted while $V_{PP} = V_{PPL}$, the V_{PP} Status bit will be set to "1".

When erase completes, the Erase Status bit should be checked. If an erase error is detected, the device's Status Register should be cleared. The CUI remains in Read Status Register mode until receiving an alternate command.

Erase Suspend (B0H)/Erase Resume (D0H)

Erase Suspend allows block erase interruption to read data from another block of the device or to temporarily conserve power for another system operation. Once the erase process starts, writing the Erase Suspend command to the CUI (see Figure 15) requests the WSM to suspend the erase sequence at a predetermined point in the erase algorithm. In the erase suspend state, the device continues to output Status Register data when read.

Polling the device's RY/$\overline{\text{BY}}$ and Erase Suspend Status bits (Status Register) will determine when the erase suspend mode is valid. It is important to note that the card's RDY/$\overline{\text{BSY}}$ pin will also transition to V_{OH} and will generate an interrupt if this pin is connected to a system-level interrupt. At this point, a Read Array command can be written to the device's CUI to read data from blocks **other than those which are suspended**. The only other valid commands at this time are Read Status Register (70H) and Erase Resume (D0H). If V_{PP} goes low during Erase Suspend, the V_{PP} Status bit is set in the Status Register and the erase operation is aborted.

The Erase Resume command clears the Erase Suspend state and allows the WSM to continue with the erase operation. The device's RY/$\overline{\text{BY}}$ Status and Erase Suspend Status bits and the card's READY-BUSY Status Register are automatically updated to reflect the erase resume condition. The card's RDY/$\overline{\text{BSY}}$ pin also returns to V_{OL}.

Invalid/Reserved

These are unassigned commands having the same effect as the Read Array command. Do not issue any command other than the valid commands specified above. Intel reserves the right to redefine these codes for future functions.

DEVICE STATUS REGISTER

Each 28F008SA device in the Series 2 Card contains a Status Register which displays the condition of its Write State Machine. The Status Register is read at any time by writing the Read Status command to the CUI. After writing this command, all subsequent Read operations output data from the Status Register, until another command is written to the CUI.

Bit 7—WSM Status

This bit reflects the Ready/Busy condition of the WSM. A "1" indicates that read, block-erase or data- write operations are available. A "0" indicates that write or erase operations are in progress.

Bit 6—Erase Suspend Status

If an Erase Suspend command is issued during the erase operation, the WSM halts execution and sets the WSM Status bit and the Erase Suspend Status bit to a "1". This bit remains set until the device receives an Erase Resume command, at which point the CUI resets the WSM Status bit and the Erase Suspend Status bit.

Bit 5—Erase Status

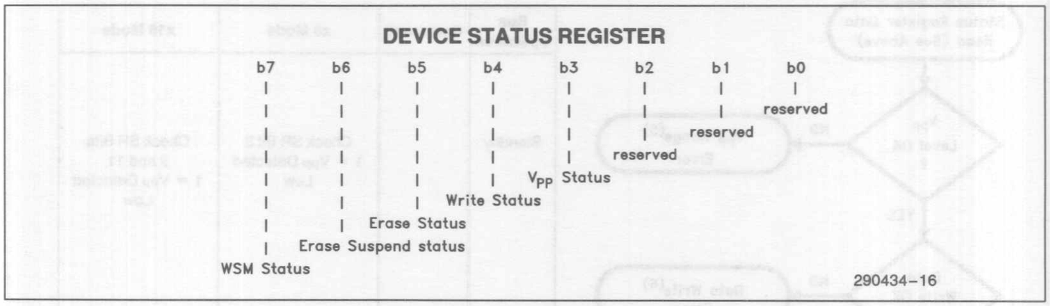
This bit will be cleared to 0 to indicate a successful block-erasure. When set to a "1", the WSM has been unsuccessful at performing an erase verification. The device's CUI only resets this bit to a "0" in response to a Clear Status Register command.

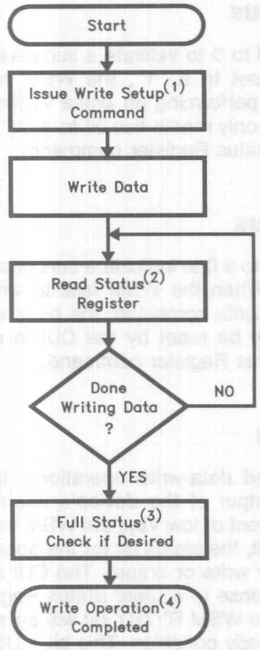
Bit 4—Write Status

This bit will be cleared to a 0 to indicate a successful data-write operation. When the WSM fails to write data after receiving a write command, the bit is set to a "1" and can only be reset by the CUI in response to a Clear Status Register command.

Bit 3—V_{PP} Status

During block-erase and data-write operations, the WSM monitors the output of the device's internal V_{PP} detector. In the event of low V_{PP}, the WSM sets ("1") the V_{PP} Status bit, the status bit for the operation in progress (either write or erase). The CUI resets these bits in response to a Clear Status Register command. Also, the WSM RY/$\overline{BY}$ bit will be set to indicate a device ready condition. This bit MUST be reset by system software (Clear Status Register command) before further data writes or block erases are attempted.

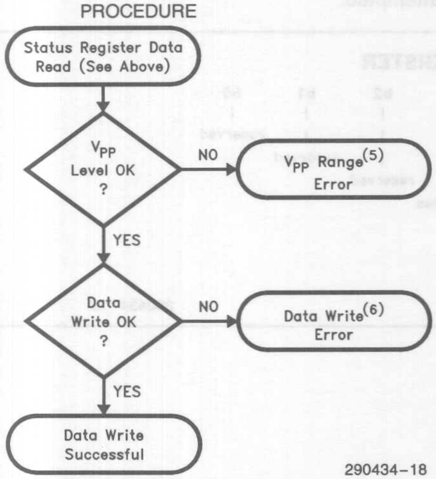




290434–17

Bus Operation	Command	x8 Mode	x16 Mode
Write	Write Setup	Data = 40H Address = Byte Within Card to be Written	Data = 4040H Address = Word Within Card to be Written
Write	Data Write	Data to be Written Address = Byte Within Card to be Written	Data to be Written Address = Word Within Card to be Written
Read	Defaults to Device Status Register Read Mode	Status Register Data. Toggle $\overline{OE}$, $\overline{CE}_1$ or $\overline{CE}_2$ to update Status Register	Status Register Data. Toggle $\overline{OE}$ or ($\overline{CE}_1$ and $\overline{CE}_2$) to update Status Registers
Standby		Check SR Bit 7 1 = Ready, 0 = Busy	Check SR Bits 7 and 15 1 = Ready, 0 = Busy

FULL STATUS CHECK PROCEDURE



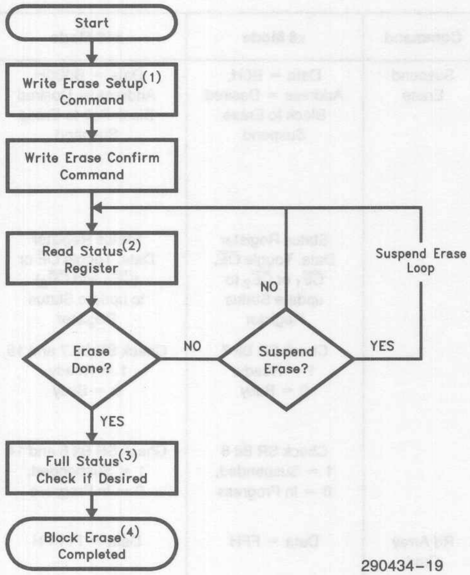
290434–18

Bus Operation	Command	x8 Mode	x16 Mode
Standby		Check SR Bit 3 1 = V_{PP} Detected Low	Check SR Bits 3 and 11 1 = V_{PP} Detected Low
Standby		Check SR Bit 4 1 = Data Write Error	Check SR Bits 4 and 12 1 = Data Write Error

Figure 13. Device-Level Automated Write Algorithm

NOTES:

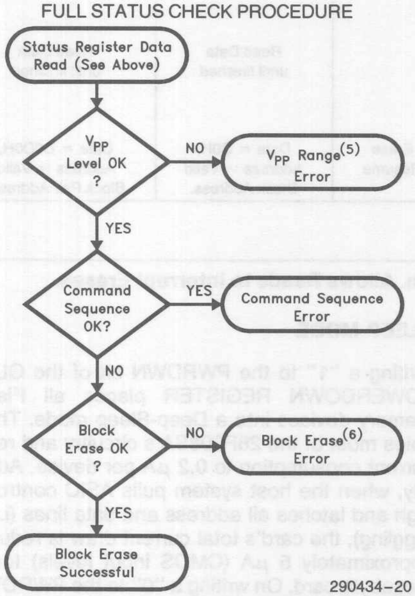
1. Repeat for subsequent data writes.
2. In addition, the card's READY-BUSY STATUS REGISTER or the RDY/$\overline{BSY}$ pin may be used.
3. Full device-level status check can be done after each data write or after a sequence of data writes.
4. Write FFH (or FFFFH) after the last data write operation to reset the device(s) to Read Array Mode.
5. If a data write operation fails due to a low V_{PP} (setting SR Bit 3), the Clear Status Register command MUST be issued before further attempts are allowed by the Write State Machine.
6. If a data write operation fails during a multiple write sequence, SR Bit 4 (Write Status) will not be cleared until the Command User Interface receives the Clear Status Register command.



Bus Operation	Command	x8 Mode	x16 Mode
Write	Erase Setup	Data = 20H Address = Block Within Card to be Erased	Data = 2020H Address = Block Pair Within Card to be Erased
Write	Erase	Data = D0H Address = Block Within Card to be Erased	Data = D0D0H Address = Block Pair Within Card to be Erased
Read	Defaults to Device Status Register Read Mode	Status Register Data. Toggle $\overline{OE}$, $\overline{CE}_1$ or $\overline{CE}_2$ to update Status Register	Status Register Data. Toggle $\overline{OE}$ or ($\overline{CE}_1$ and $\overline{CE}_2$) to update Status Register
Standby		Check SR Bit 7 1 = Ready, 0 = Busy	Check SR Bits 7 and 15 1 = Ready, 0 = Busy

290434–19

FULL STATUS CHECK PROCEDURE

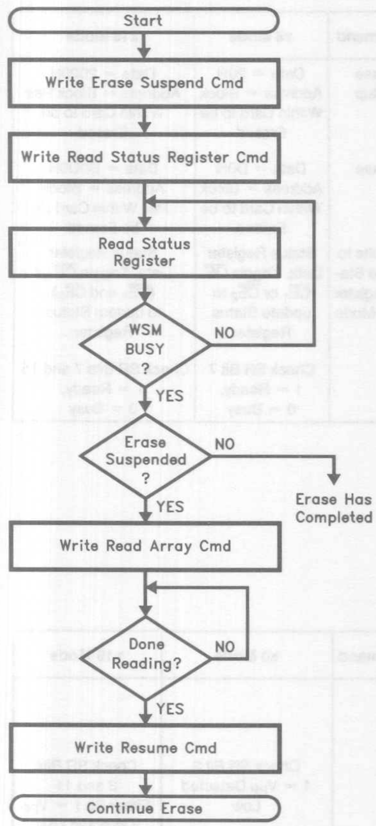


Bus Operation	Command	x8 Mode	x16 Mode
Standby		Check SR Bit 3 1 = V_{PP} Detected Low	Check SR Bits 3 and 11 Either Bit 1 = V_{PP} Detected Low
Standby		Check SR Bits 4 and 5 Both 1 = Command Sequence Error	Check SR Bits 4, 5, 12, 13 All 1 = Command Sequence Error
Standby		Check SR Bit 5 1 = Block Erase Error	Check SR Bits 5 and 13 Both 1 = Block Erase Failure

290434–20

Figure 14. Device-Level Automated Erase Algorithm

NOTES:
1. Repeat for subsequent data writes.
2. In addition, the card's READY-BUSY STATUS REGISTER or the RDY/$\overline{BSY}$ pin may be used.
3. Full device-level status check can be done after each block erase or after a sequence of block erases.
4. Write FFH (or FFFFH) after the last block erase operation to reset the device(s) to Ready Array Mode.
5. If a block erase operation fails due to a low V_{PP} (setting SR Bit 3), the Clear Status Register command MUST be issued before further attempts are allowed by the Write State Machine.
6. If a block erase operation fails during a multiple block erase sequence, SR Bit 4 (Write Status) will not be cleared until the Command User Interface receives the Clear Status Register command.



290434-27

Bus Operation	Command	x8 Mode	x16 Mode
Write	Suspend Erase	Data = B0H, Address = Desired Block to Erase Suspend	Data = B0B0H, Address = Desired Block Pair to Erase Suspend
Read		Status Register Data. Toggle $\overline{OE}$, $\overline{CE}_1$ or $\overline{CE}_2$ to update Status Register	Status Register Data. Toggle $\overline{OE}$ or ($\overline{CE}_1$ and $\overline{CE}_2$) to update Status Register
Standby		Check SR Bit 7 1 = Ready, 0 = Busy	Check SR Bit 7 and 15 1 = Ready, 0 = Busy
Standby		Check SR Bit 6 1 = Suspended, 0 = In Progress	Check SR Bit 6 and 14 1 = Suspended, 0 = In Progress
Write	Rd Array Cmd	Data = FFH	Data = FFFFH
Read		Read Data until finished	Read Data until finished
Write	Erase Resume	Data = D0H, Address = Valid Block Address.	Data = D0D0H, Address = Valid Block Pair Address.

Figure 15. Erase Suspend/Resume Algorithm. Allows Reads to Interrupt Erases.

POWER CONSUMPTION

STANDBY MODE

In most applications, software will only be accessing one device pair at a time. The Series 2 Card is defined to be in the standby mode when one device pair is in the Read Array Mode while the remaining devices are in the Deep-Sleep Mode. The Series 2 Card's $\overline{CE}_1$ and $\overline{CE}_2$ input signals must also be at V_{IH}. In standby mode, much of the card's circuitry is shut off, substantially reducing power consumption. Typical power consumption for a 20 Megabyte Series 2 card in standby mode is 65 μA.

SLEEP MODE

Writing a "1" to the PWRDWN bit of the GLOBAL POWERDOWN REGISTER places all FlashFile Memory devices into a Deep-Sleep mode. This disables most of the 28F008SA's circuitry and reduces current consumption to 0.2 μA per device. Additionally, when the host system pulls ASIC control logic high and latches all address and data lines (i.e., not toggling), the card's total current draw is reduced to approximately 5 μA (CMOS input levels) for a 20 Megabyte card. On writing a "0" to the PWRDWN bit (Global PowerDown Register) or any individual device pair (Sleep Control Register), a Deep-Sleep mode recovery period must be allowed for 28F008SA device circuitry to power back on.

SYSTEM DESIGN CONSIDERATIONS

POWER SUPPLY DECOUPLING

Flash memory power-switching characteristics require careful device decoupling. System designers are interested in three supply current issues—standby, active and transient current peaks, produced by rising and falling edges of CE_1 and CE_2. The capacitive and inductive loads on the card and internal flash memory device pairs determine the magnitudes of these peaks.

The Flash Memory Card features on-card ceramic decoupling capacitors connected between V_{CC} and GND, and between V_{PP1}/V_{PP2} and GND to help transient voltage peaks.

On the host side, the card connector should also have a 4.7 μF electrolytic capacitor between V_{CC} and GND, as well as between V_{PP1}/V_{PP2} and GND. The bulk capacitors will overcome voltage slumps caused by printed-circuit-board trace inductance, and will supply charge to the smaller capacitors as needed.

POWER UP/DOWN PROTECTION

Each device in the Flash Memory Card is designed to offer protection against accidental erasure or writing, caused by spurious system-level signals that may exist during power transitions. The card will power-up into the Read Array Mode.

A system designer must guard against active writes for V_{CC} voltages above V_{LKO} when V_{PP} is active. Since both $\overline{WE}$ and $\overline{CE}_1$ (and/or $\overline{CE}_2$) must be low for a command write, driving either to V_{IH} will inhibit writes. With its Command User Interface, alteration of device contents only occurs after successful completion of the two-step command sequences.

While these precautions are sufficient for most applications, an alternative approach would allow V_{CC} to reach its steady state value before raising V_{PP1}/V_{PP2} above V_{CC} + 2.0V. In addition, upon powering-down, V_{PP1}/V_{PP2} should be below V_{CC} + 2.0V, before lowering V_{CC}.

HOT INSERTION/REMOVAL

The capability to remove or insert PC cards while the system is powered on (i.e., hot insertion/removal) requires careful design approaches on the system and card levels. To design for this capability consider card overvoltage stress, system power droop and control line stability.

A PCMCIA/JEIDA specified socket properly sequences the power supplies to the flash memory card via shorter and longer pins. This assures that hot insertion and removal will not result in card damage or data loss.

PCMCIA CARD INFORMATION STRUCTURE

The Card Information Structure (CIS) starts at address zero of the card's Attribute Memory Plane. It contains a variable-length chain of data blocks (tuples) that conform to a basic format as shown in Table 5. This section describes each tuple contained within the Series 2 Flash Memory Card.

The Device Information Tuple

This tuple (CISTPL__DEV = 01H) contains information pertaining to the card's speed and size. The Series 2 Card is offered with a 200 or 250 nanosecond access time. Card sizes range between 2 and 20 Megabytes.

Table 5. Tuple Format

Bytes	Data
0	Tuple Code: CISTPL__xxx. The tuple code 0FFH indicates no more tuples in the list.
1	Tuple Link: TPL__LINK. Link to the next tuple in the list. This can be viewed as the number of additional bytes in tuple, excluding this byte. If the link field is zero, the tuple body is empty. If the link field contains 0FFH, this tuple is the last tuple in the list.
2–n	Bytes specific to this tuple.

The Device Geometry Tuple

This tuple (CISTPL_DEVICEGEO = 1EH) is conceptually similar to a DOS disk geometry tuple (CISTPL_GEOMETRY), except it is not a format-dependent property; this deals with the fixed architecture of the memory device(s).

Fields are defined as follows:

DGTPL BUS—Value = n, where system bus width = $2^{(n-1)}$ bytes. N = 2 for standard PCMCIA Release 1.0/2.0 cards.

DGTPL EBS—Value = n, where the memory array's physical memory segments have a minimum erase block size of $2^{(n-1)}$ address increments of DGTPL_BUS-wide accesses.

DGTPL RBS—Value = n, where the memory array's physical memory segments have a minimum read block size of $2^{(n-1)}$ address increments of DGTPL_BUS-wide accesses.

DGTPL WBS—Value = n, where the memory array's physical memory segments have a minimum write block size of $2^{(n-1)}$ address increments of DGTPL_BUS-wide accesses.

DGTPL PART—Value = n, where the memory array's physical memory segments can have partitions subdividing the arrays in minimum granularity of $2^{(n-1)}$ number of erase blocks.

FL DEVICE INTERLEAVE—Value = n, where card architectures employ a multiple of $2^{(n-1)}$ times interleaving of the entire memory arrays with the above characteristics. Non-interleaved cards have values n = 1.

Jedec Programming Information Tuple

This tuple (CISTPL_JEDEC = 18H) contains the Intel manufacturing identifier (89H) and the 28F008SA device ID (A2H).

Level 1 Version/Product Information Tuple

This tuple (CISTPL_VERI = 15H) contains Level-1-version compliance and card-manufacturer information. Fields are described as follows:

TPLLV1 MAJOR—Major version number = 04H.

TPLLV1 MINOR—Minor version number = 01H for release 2.0.

TPLLV1 INFO—

Name of manufacturer	= intel;
Name of product	SERIES2-"Card size";
Card type	= 2;
Speed	= 150 ns or 200 ns
Register Base	= REGBASE 4000H
Test Codes	= DBBDRELP
Legalities	= COPYRIGHT intel Corporation 1991

The Configurable Card Tuple

This tuple (CISTPL_CONF = 1AH) describes the interface supported by the card and the locations of the Card Configuration Registers and the Card Configuration Table.

Fields are described as follows:

TPCC SZ—Size of fields byte = 01H.

TPCC LAST—Index number of the last entry in the Card Configuration Table = 00H.

TPCC RADR—Configuration Registers Base Address in Reg Space = 4000H.

TPCC RMSK—Configuration Registers Present Mask = 03H.

The End-Of-List Tuple

The end-of-list tuple (CISTPL_END = FFH) marks the end of a tuple chain. Upon encountering this tuple, continue tuple processing as if a long-link to address 0 of common memory space were encountered.

Tuple Address	Value	Description
00H	01H	CISTPL__DEV
02H	03H	TPL__LINK
04H	53H 52H	DEVICE__INFO = FLASH 150 ns DEVICE__INFO = FLASH 200 ns
06H	06H 0EH 26H 4EH	CARD SIZE 2M 4M 10M 20M
08H	FFH	END OF DEVICE
0AH	1EH	CISTPL__ DEVICEGEO
0CH	06H	TPL__LINK
0EH	02H	DGTPL__BUS
10H	11H	DGTPL__EBS
12H	01H	DGTPL__RBS
14H	01H	DGPL__WBS
16H	03H	DGTPL__PART
18H	01H	FL__DEVICE INTERLEAVE
1AH	18H	CISTPL__JEDEC
1CH	02H	TPL__LINK
1EH	89H	INTEL J-ID
20H	A2H	28F008 J-ID
22H	15H	CISTPL__VER1
24H	50H	TPL__LINK
26H	04H	TPLLV1 MAJOR
28H	01H	TPLLV1 MINOR
2AH	69H	TPLLV1 INFO i
2CH	6EH	n
2EH	74H	t
30H	65H	e

Tuple Address	Value	Description
32H	6CH	l
34H	00H	END TEXT
36H	53H	S
38H	45H	E
3AH	52H	R
3CH	49H	I
3EH	45H	E
40H	53H	S
42H	32H	2
44H	2DH	—
46H	30H 30H 31H 32H	2M = 0 4M = 0 10M = 1 20M = 2
48H	32H 34H 30H 30H	2M = 2 4M = 4 10M = 0 20M = 0
4AH	20H	SPACE
4CH	00H	END TEXT
4EH	32H	CARD TYPE 2
50H	41H 42H 45H 5AH 48H 49H 4CH 4FH	A = 2M, 150 ns B = 4M, 150 ns E = 10M, 150 ns Z = 20M, 150 ns H = 2M, 200 ns I = 4M, 200 ns L = 10M, 200 ns O = 20M, 200 ns

Tuple Address	Value	Description
52H	20H	SPACE
54H	52H	REGBASE-R
56H	45H	E
58H	47H	G
5AH	42H	B
5CH	41H	A
5EH	53H	S
60H	45H	E
62H	20H	SPACE
64H	34H	4000h 4
66H	30H	0
68H	30H	0
6AH	30H	0
6CH	68H	h
6EH	20H	SPACE
70H	44H	D
72H	42H	B
74H	42H	B
76H	44H	D
78H	52H	R
7AH	45H	E
7CH	4CH	L
7EH	50H	P
80H	00H	END TEXT
82H	43H	COPYRIGHT C
84H	4FH	O
86H	50H	P
88H	59H	Y
8AH	52H	R
8CH	49H	I
8EH	47H	G
90H	48H	H
92H	54H	T
94H	20H	SPACE

Tuple Address	Value	Description
96H	69H	i
98H	6EH	n
9AH	74H	t
9CH	65H	e
9EH	6CH	l
AoH	20H	SPACE
A2H	43H	CORPORATION C
A4H	4FH	O
A6H	52H	R
A8H	50H	P
AAH	4FH	O
ACH	52H	R
AEH	41H	A
B0H	54H	T
B2H	49H	I
B4H	4FH	O
B6H	4EH	N
B8H	20H	SPACE
BAH	31H	1
BCH	39H	9
BEH	39H	9
C0H	31H	1
C2H	00H	END TEXT
C4H	FFH	END OF LIST
C6H	1AH	CISTPL_CONF
C8H	06H	TPL_LINK
CAH	01H	TPCC_SZ
CCH	00H	TPCC_LAST
CEH	00H	TPCC_RADR
D0H	40H	TPCC_RADR
D2H	03H	TPCC_RMSK
D4H	FFH	END OF LIST
D6H	FFH	CISTPL_END
D8H	00H	INVALID ECIS ADDRESS

OPERATING SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature
During Read .... 0°C to +60°C(1)
During Erase/Write .... 0°C to +60°C

Storage Temperature .... −30°C to +70°C

Voltage on Any Pin with
Respect to Ground .... −2.0V to +7.0V(2)

V_{PP1}/V_{PP2} Supply Voltage with
Respect to Ground
during Erase/Write .... −2.0V to +14.0V(2, 3)

V_{CC} Supply Voltage with
Respect to Ground .... −0.5V to +6.0V

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

***WARNING:** *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

NOTES:
1. Operating temperature is for commercial product defined by this specification.
2. Minimum DC input voltage is −0.5V. During transitions, inputs may undershoot to −2.0V tor periods less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5V, which may overshoot to V_{CC} + 2.0V for periods less than 20 ns.
3. Maximum DC input voltage on V_{PP1}/V_{PP2} may overshoot to +14.0V tor periods less than 20 ns.

OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
T_A	Operating Temperature	0	60	°C
V_{CC}	V_{CC} Supply Voltage (5%)	4.75	5.25	V

COMMON DC CHARACTERISTICS, CMOS and TTL

Symbol	Parameter	Notes	Min	Typ	Max	Unit	Test Condition
I_{LI}	Input Leakage Current	1, 3		±1	±20	μA	$V_{CC} = V_{CC}$ Max $V_{IN} = V_{CC}$ or GND
I_{LO}	Output Leakage Current	1		±1	±20	μA	$V_{CC} = V_{CC}$ Max $V_{OUT} = V_{CC}$ or GND
V_{IL}	Input Low Voltage	1	−0.5		0.8	V	
V_{IH}	Input High Voltage (TTL)	1	2.4		V_{CC} + 0.3	V	
	Input High Voltage (CMOS)		0.7 V_{CC}		V_{CC} + 0.3		
V_{OL}	Output Low Voltage	1	V_{SS}		0.4	V	$V_{CC} = V_{CC}$ Min I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	1	4.0		V_{CC}	V	$V_{CC} = V_{CC}$ Min I_{OH} = 2.0 mA
V_{PPL}	V_{PP} during Read Only Operations	1, 2	0.0		6.5	V	
V_{PPH}	V_{PP} during Read/Write Operations	1	11.4		12.6	V	
V_{LKO}	V_{CC} Erase/Write Lock Voltage	1	2.0			V	

NOTES:
1. Values are the same for byte and word wide modes and for all card densities.
2. Block Erases/Data Writes are inhibited when V_{PP} and V_{PPL} and not guaranteed in the range between V_{PPH} and V_{PPL}.
3. Exceptions: With V_{IN} = GND, the leakage on $\overline{CE}_1$, $\overline{CE}_2$, $\overline{REG}$, $\overline{OE}$, $\overline{WE}$, will be ≤ 500 μA due to internal pullup resistors and, with $V_{IN} = V_{CC}$, RST leakage will be ≤ 500 μA due to internal pulldown resistor.

DC CHARACTERISTICS, CMOS

Symbol	Parameter		Notes	Byte Wide Mode			Word Wide Mode			Unit	Test Condition
				Min	Typ	Max	Min	Typ	Max		
I_{CCR}	V_{CC} Read Current		1, 3		45	85		65	120	mA	$V_{CC} = V_{CC}$ Max, Control Signals = GND, t_{CYCLE} = 200 ns, I_{OUT} = 0 mA
I_{CCW}	V_{CC} Write Current		1, 3		35	80		45	110	mA	Data Write in Progress
I_{CCE}	V_{CC} Erase Current		1, 2, 3		35	80		45	110	mA	Block (Pair) Erase in Progress
I_{CCS}	V_{CC} Standby Current	4 Meg			61	222		61	222		$V_{CC} = V_{CC}$ Max, Control Signals $= V_{IH}$
		10 Meg	1, 4, 6		63	230		63	230	μA	
		20 Meg			65	242		65	242		
I_{CCSL}	V_{CC} Sleep Current	4 Meg			2	25		2	25		
		10 Meg	1, 4, 5		3	32		3	32	μA	
		20 Meg			5	44		5	44		
I_{PPW}	V_{PP} Write Current ($V_{PP} = V_{PPH}$)		1, 3		10	30		20	60	mA	Data Write in Progress
I_{PPE}	V_{PP} Erase Current ($V_{PP} = V_{PPH}$)		1, 3		10	30		20	60	mA	Block (Pair) Erase in Progress
I_{PPSL}	V_{PP} Sleep Current	4 Meg			0.5	4		0.5	4		
		10 Meg	1, 5		1	10		1	10	μA	
		20 Meg			2	20		2	20		
I_{PPS1}	V_{PP} Standby or Read Current ($V_{PP} \leq V_{CC}$)	4 Meg			1.5	13		1.5	13		
		10 Meg	1, 6		2	19		2	19	μA	
		20 Meg			3	29		3	29		
I_{PPS2}	V_{PP} Standby or Read Current ($V_{PP} = V_{PPH}$)	4 Meg			90	203		180	402		
		10 Meg	1, 6		91	209		181	408	μA	
		20 Meg			92	219		182	418		

NOTES:

1. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 5.0V, V_{PP} = 12.0V, T = 25°C.
2. The Data Sheet specification for the 28F008SA in Erase Suspend (I_{CCES}) is 5 mA typical and 10 mA max with the device deselected. If the device(s) are read while in Erase Suspend Mode, current draw is the sum of I_{CCES} and I_{CCR}.
3. Standby or Sleep currents are not included for non-accessed devices.
4. Address and data inputs to card static. Control line voltages equal to V_{IH} or V_{IL}.
5. All 28F008SA devices in Deep-Sleep (PowerDown) mode.
6. In Byte and Word Mode, all but two devices in Deep-Sleep.

DC CHARACTERISTICS, TTL

Symbol	Parameter		Notes	Byte Wide Mode Min	Byte Wide Mode Typ	Byte Wide Mode Max	Word Wide Mode Min	Word Wide Mode Typ	Word Wide Mode Max	Unit	Test Condition
I_{CCR}	V_{CC} Read Current		1, 3		75	150		100	200	mA	$V_{CC} = V_{CC}$ Max, $t_{CYCLE} = 200$ ns, $I_{OUT} = 0$ mA
I_{CCW}	V_{CC} Write Current		1, 3		60	130		70	160	mA	Data Write in Progress
I_{CCE}	V_{CC} Erase Current		1, 2, 3		60	130		70	160	mA	Block (Pair) Erase in Progress
I_{CCS}	V_{CC} Standby Current	4 Meg	1, 4, 6, 7								$V_{CC} = V_{CC}$ Max, Control Signals $= V_{IH}$
		10 Meg			20	100		20	100	mA	
		20 Meg									
I_{CCSL}	V_{CC} Sleep Current	4 Meg	1, 4, 5, 7								
		10 Meg			20	100		20	100	mA	
		20 Meg									
I_{PPW}	V_{PP} Write Current ($V_{PP} = V_{PPH}$)		1, 3		10	30		20	60	mA	Data Write in Progress
I_{PPE}	V_{PP} Erase Current ($V_{PP} = V_{PPH}$)		1, 3		10	30		20	60	mA	Block (Pair) Erase in Progress
I_{PPSL}	V_{PP} Sleep Current	4 Meg	1, 5		3	20		3	20	μA	
		10 Meg			8	50		8	50		
		20 Meg			16	100		16	100		
I_{PPS1}	V_{PP} Standby or Read Current ($V_{PP} \leq V_{CC}$)	4 Meg	1, 6		3	25		3	25	μA	
		10 Meg			8	55		8	55		
		20 Meg			16	105		16	105		
I_{PPS2}	V_{PP} Standby or Read Current ($V_{PP} = V_{PPH}$)	4 Meg	1, 6		92	215		182	410	μA	
		10 Meg			97	245		186	440		
		20 Meg			105	295		194	490		

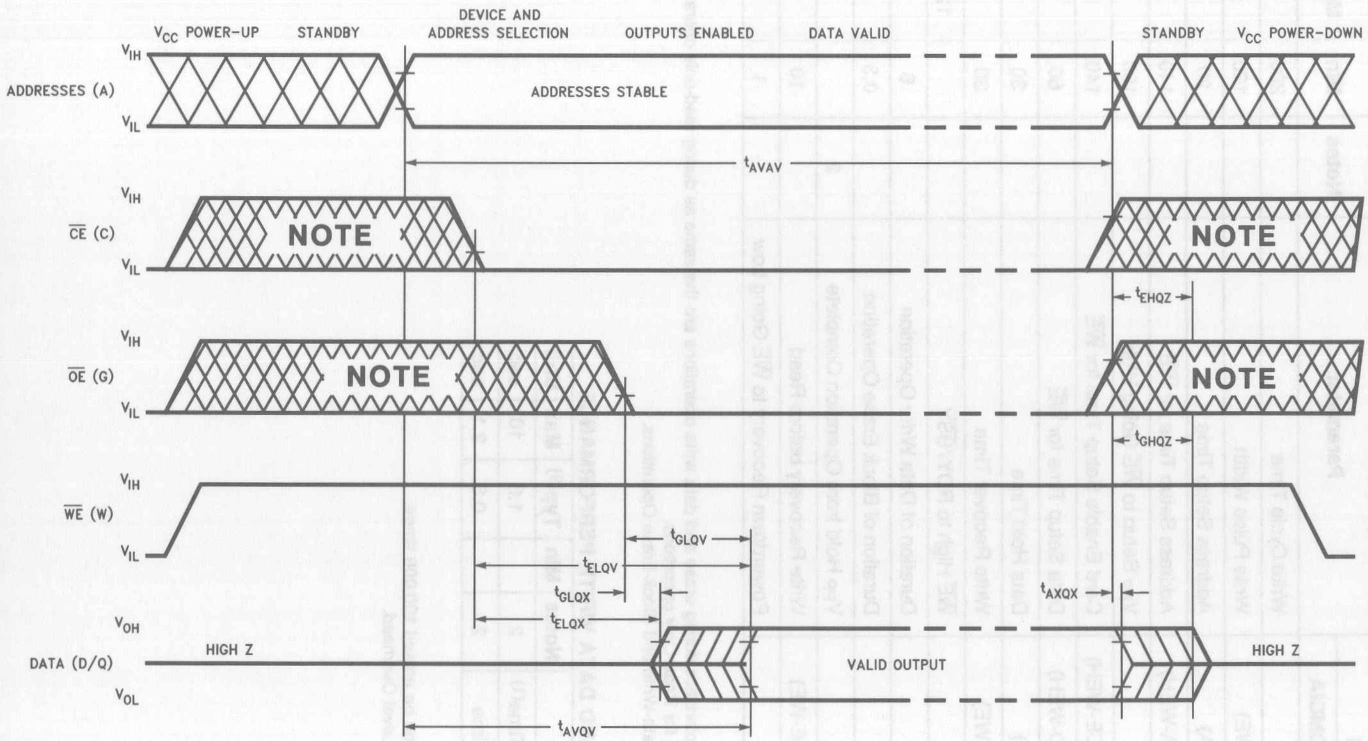
NOTES:
1. All currents are in RMS unless otherwise noted. Typical values at $V_{CC} = 5.0V$, $V_{PP} = 12.0V$, $T = 25°C$.
2. The Data Sheet specification for the 28F008SA in Erase Suspend (I_{CCES}) is 5 mA typical and 10 mA max with the device deselected. If the device(s) are read while in Erase Suspend Mode, current draw is the sum of I_{CCES} and I_{CCR}.
3. Standby or Sleep currents are not included for non-accessed devices.
4. Address and data inputs to card static. Control line voltages equal to V_{IH} or V_{IL}.
5. All 28F008SA devices in Deep-Sleep (PowerDown) mode.
6. In Byte and Word Mode, all but two devices in Deep-Sleep.
7. The current consumption from the 28F008SA is insignificant in relation to the ASIC's.

AC CHARACTERISTICS

AC Timing Diagrams and characteristics are guaranteed to meet or exceed PCMCIA Release 2.0 specifications. PCMCIA allows a 300 ns access time for Attribute Memory. Note that read and write access timings to the Series 2 Flash Memory Card's Common and Attribute Memory Planes are identical at 200 ns. Furthermore, there is no delay in switching between the Common and Attribute Memory Planes.

COMMON AND ATTRIBUTE MEMORY, AC CHARACTERISTICS: Read-Only Operations

Symbol		Parameter	Notes	Min	Max	Unit
JEDEC	PCMCIA					
t_{AVAV}	t_{RC}	Read Cycle Time		200		ns
t_{AVQV}	t_a (A)	Address Access Time			200	ns
t_{ELQV}	t_a (CE)	Card Enable Access Time			200	ns
t_{GLQV}	t_a (OE)	Output Enable Access Time			100	ns
t_{EHQX}	t_{dis} (CE)	Output Disable Time from $\overline{CE}$			90	ns
t_{GHQZ}	t_{dis} (CE)	Output Disable Time from $\overline{OE}$			70	ns
t_{GLQX}	t_{en} (CE)	Output Enable Time from $\overline{CE}$		5		ns
t_{ELQX}	t_{en} (OE)	Output Enable Time from $\overline{OE}$		5		ns
t_{AXQX}	t_v (A)	Data Valid from Add Change		0		ns
t_{PHQV}		Powerdown Recovery to Output Delay		500		ns
	t_{su} (V_{CC})	CE Setup Time on Power-Up		1		ms
		First Access after Reset		500		ns



NOTE:
1. The hatched area may be either high or low.

Figure 16. AC Waveform for Read Operations

COMMON AND ATTRIBUTE MEMORY, AC CHARACTERISTICS: Write Operations[1]

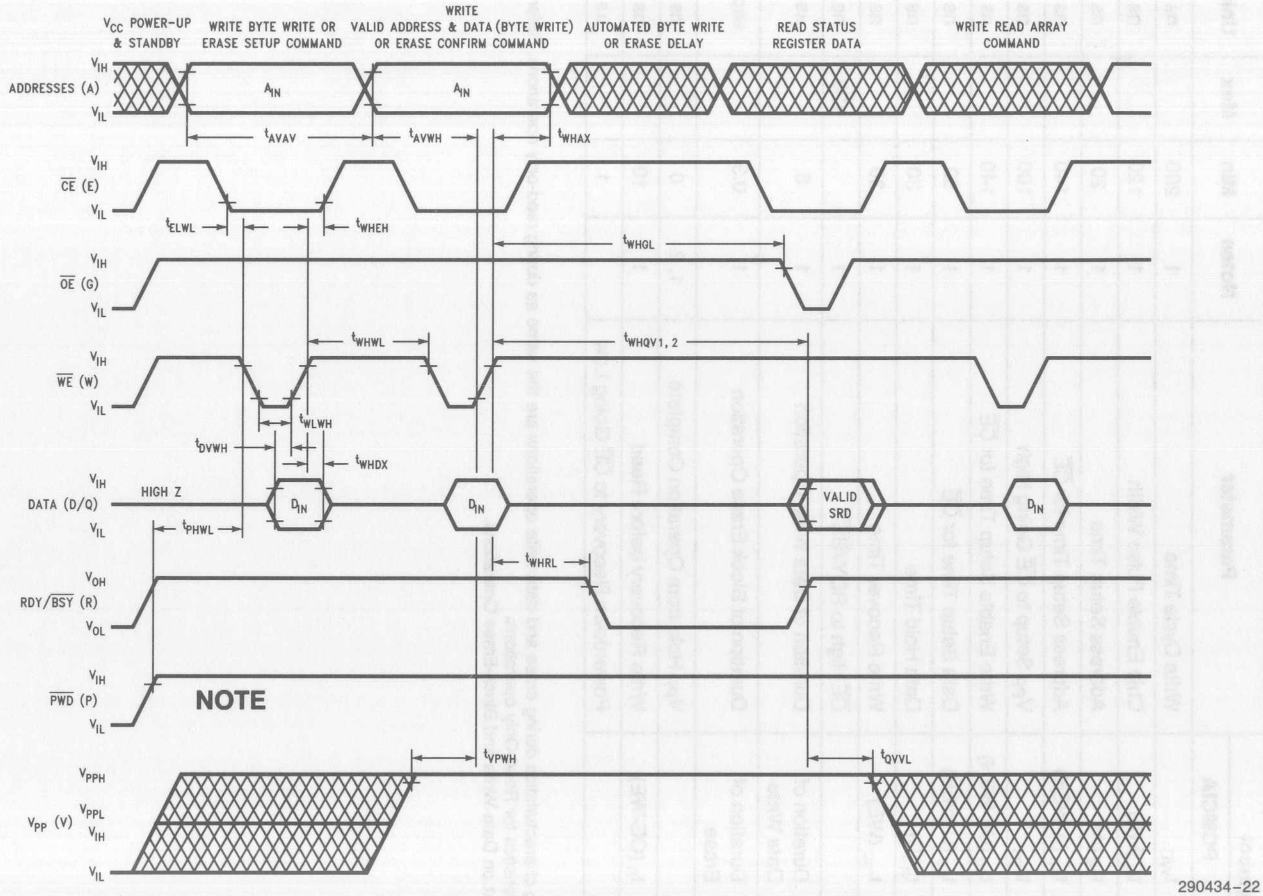
Symbol		Parameter	Notes	Min	Max	Unit
JEDEC	PCMCIA					
t_{AVAV}	t_{WC}	Write Cycle Time		200		ns
t_{WLWH}	t_w (WE)	Write Pulse Width		120		ns
t_{AVWL}	t_{su} (A)	Address Setup Time		20		ns
t_{AVWH}	t_{su} (A-WEH)	Address Setup Time for $\overline{WE}$		140		ns
t_{VPWH}	t_{vps}	V_{PP} Setup to $\overline{WE}$ Going High		100		ns
t_{ELWH}	t_{su} (CE-WEH)	Card Enable Setup Time for $\overline{WE}$		140		ns
t_{DVWH}	t_{su} (D-WEH)	Data Setup Time for $\overline{WE}$		60		ns
t_{WHDX}	t_h (D)	Data Hold Time		30		ns
t_{WHAX}	t_{rec} (WE)	Write Recover Time		30		ns
t_{WHRL}		$\overline{WE}$ High to RDY/$\overline{BSY}$			120	ns
t_{WHQV1}		Duration of Data Write Operation		6		μs
t_{WHQV2}		Duration of Block Erase Operation		0.3		sec
t_{QVVL}		V_{PP} Hold from Operation Complete	2			ns
t_{WHGL}	t_h (OE-WE)	Write Recovery before Read		10		ns
t_{PHWL}		Powerdown Recovery to $\overline{WE}$ Going Low		1		μs

NOTES:
1. Read timing characteristics during erase and data write operations are the same as during read-only operations. Refer to AC Characteristics for Read-Only operations.
2. Refer to text on Data-Write and Block-Erase Operations.

BLOCK ERASE AND DATA WRITE PERFORMANCE

Parameter	Notes	Min	Typ[3]	Max	Unit
Block Pair Erase Time[1]	2		1.6	10	sec
Block Pair Write Time	2		0.6	2.1	sec

NOTES:
1. Individual blocks can be erased 100,000 times.
2. Excludes System-Level Overhead.
3. 25°C, 12.0 V_{PP}.



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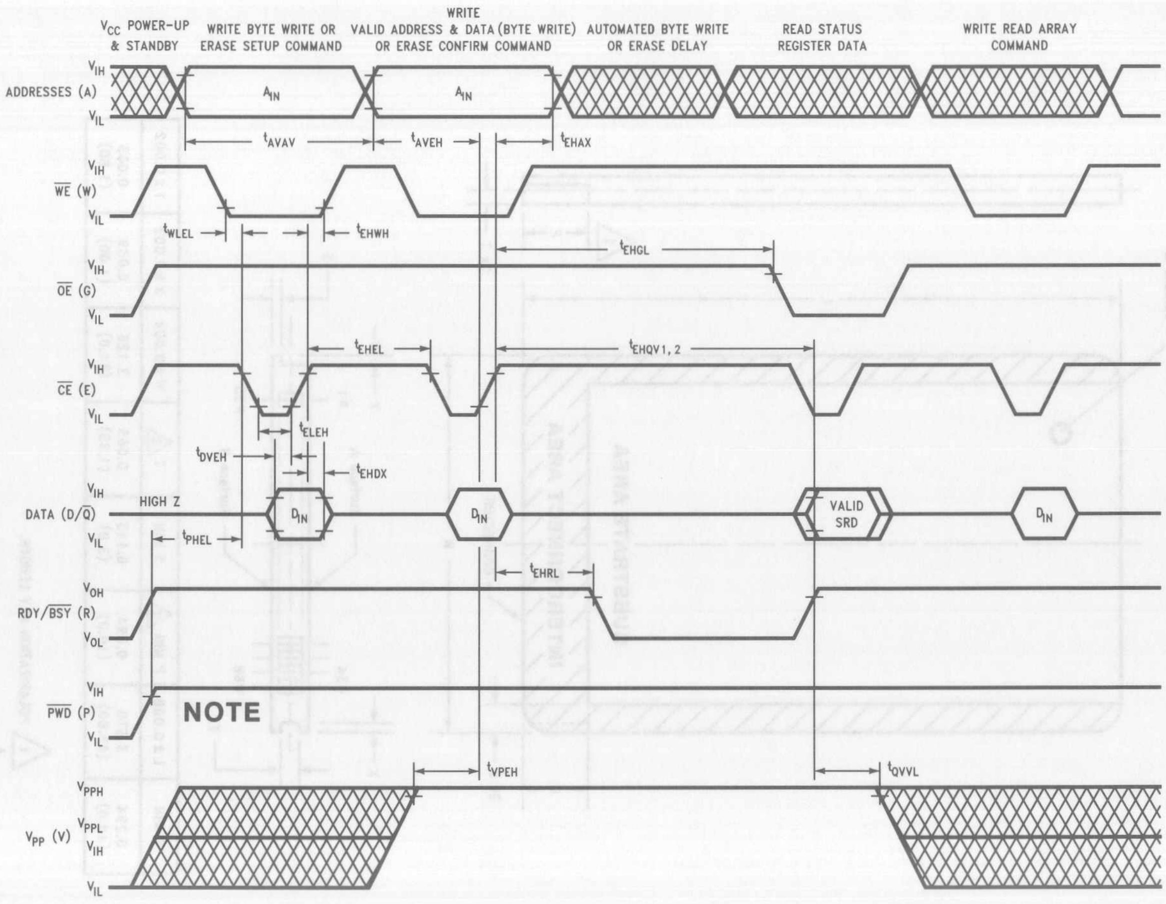
NOTE:
As shown, PWD is a carry-over from the component-level diagram; this signal is generated in the card by the ASIC by writing to the appropriate register.

Figure 17. AC Waveform for Write Operations

COMMON AND ATTRIBUTE MEMORY, AC CHARACTERISTICS: $\overline{CE}$-Controlled Write Operations(1)

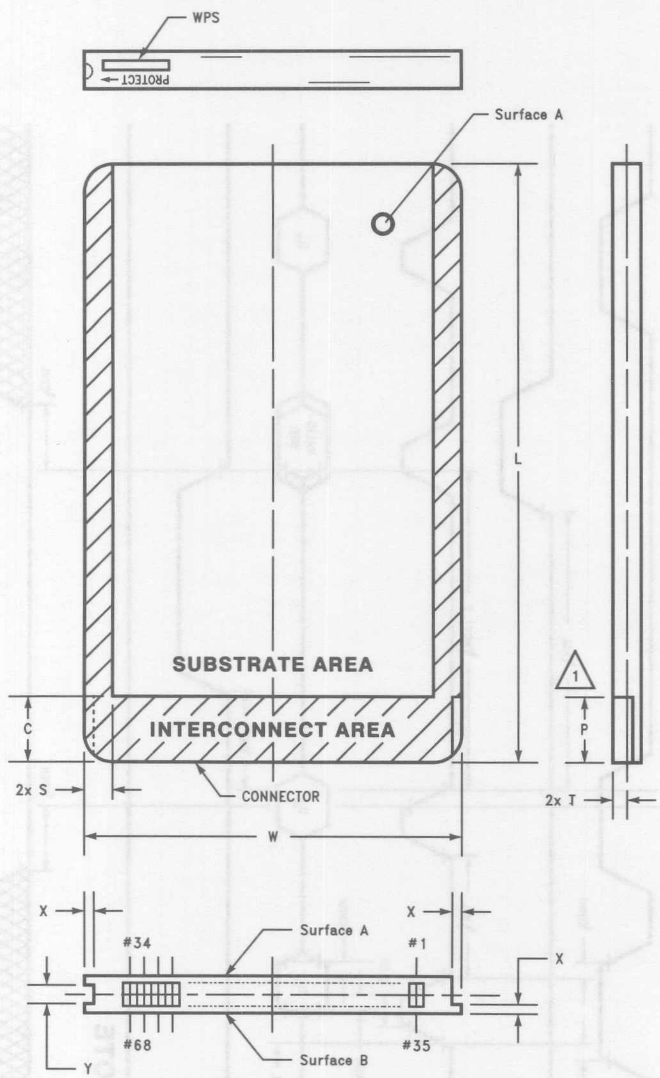
Symbol		Parameter	Notes	Min	Max	Unit
JEDEC	PCMCIA					
t_{AVAV}	t_{WC}	Write Cycle Time	1	200		ns
t_{ELEH}	t_w (WE)	Chip Enable Pulse Width	1	120		ns
t_{AVEL}	t_{su} (A)	Address Setup Time	1	20		ns
t_{AVEH}	t_{su} (A-WEH)	Address Setup Time for $\overline{CE}$	1	140		ns
t_{VPEH}	t_{vps}	V_{PP} Setup to $\overline{CE}$ Going High	1	100		ns
t_{WLEH}	t_{su} (CE-WEH)	Write Enable Setup Time for $\overline{CE}$	1	140		ns
t_{DVEH}	t_{su} (D-WEH)	Data Setup Time for $\overline{CE}$	1	60		ns
t_{EHDX}	t_h (D)	Data Hold Time	1	30		ns
t_{EHAX}	t_{rec} (WE)	Write Recover Time	1	30		ns
t_{EHRL}		$\overline{CE}$ High to RDY/$\overline{BSY}$	1		120	ns
t_{EHQV1}	Duration of Data Write	Duration of Data Write Operation	1	6		µs
t_{EHQV2}	Duration of Erase	Duration of Block Erase Operation	1	0.3		sec
t_{QVVL}		V_{PP} Hold from Operation Complete	1, 2	0		ns
t_{EHGL}	t_h (OE-WE)	Write Recovery before Read	1	10		ns
t_{PHEL}		Powerdown Recovery to $\overline{CE}$ Going Low		1		µs

NOTES:
1. Read timing characteristics during erase and data write operations are the same as during read-only operations. Refer to AC Characteristics for Read-Only operations.
2. Refer to text on Data-Write and Block-Erase Operations.



NOTE:
As shown, $\overline{PWD}$ is a carry-over from the component-level diagram; this signal is generated in the card by the ASIC by writing to the appropriate register.

Figure 18. Alternate AC Waveform for Write Operations



C MIN	L ± 0.008	P MIN ⚠1	S MIN	T ⚠2	W ± 0.004	X ± 0.002	Y ± 0.002
0.294 (10.0)	3.370 (85.60)	0.394 (10.0)	0.118 (3.0)	0.065 (1.65)	2.126 (54.0)	0.039 (1.00)	0.063 (1.60)

1. POLARIZATION KEY LENGTH.
2. INTERCONNECT AREA TOLERANCE = ±0.002
   SUBSTRATE AREA TOLERANCE = ±0.004
3. MILLIMETERS ARE IN PARENTHESIS ().

290434–24

Figure 19. Series 2 Flash Memory Card Package Dimensions

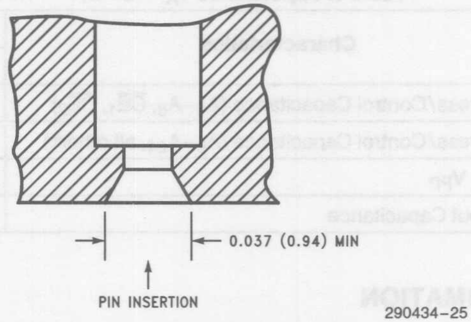
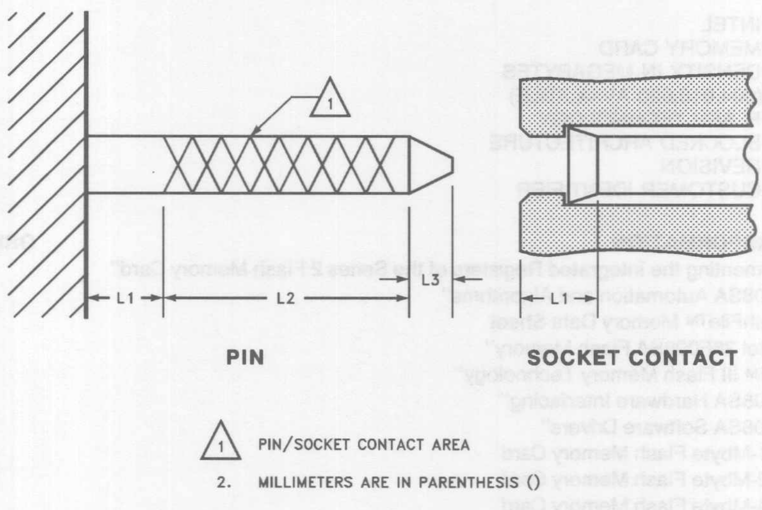


Figure 20. Card Connector Socket



L1 MAX	L2		L3 REF
0.020 (0.5)	Pin Type—See Table 1		0.024 (0.6)
	Detect	0.059 (1.5) ±0.039	
	General	0.084 (2.1) ±0.064	
	Power	0.098 (2.5) ±0.078	

Figure 21. Pin/Socket Contact Length with Wipe

Table 5. Capacitance $T_A = 25°C$, f = 1.0 MHz

Symbol	Characteristics	Commercial		Unit
		Min	Max	
C_{IN}	Address/Control Capacitance (A_0–A_8, $\overline{CE}_1$, $\overline{CE}_2$)		30	pF
	Address/Control Capacitance (A_9–A_{24}, all others)		20	pF
	V_{CC}, V_{PP}		2	μF
C_{OUT}	Output Capacitance		20	pF

ORDERING INFORMATION

iMC020FLSA,SBXXXXX

WHERE:

i	= INTEL
MC	= MEMORY CARD
020	= DENSITY IN MEGABYTES (004,010,020 AVAILABLE)
FL	= FLASH TECHNOLOGY
S	= BLOCKED ARCHITECTURE
A	= REVISION
SBXXXXX	= CUSTOMER IDENTIFIER

ADDITIONAL INFORMATION	ORDER NUMBER
AP-361 "Implementing the Integrated Registers of the Series 2 Flash Memory Card"	292096
AP-364 "28F008SA Automation and Algorithms"	292099
28F008SA FlashFile™ Memory Data Sheet	290429
ER-27 "The Intel 28F008SA Flash Memory"	294011
ER-28 "ETOX™ III Flash Memory Technology"	294012
AP-359 "28F008SA Hardware Interfacing"	292094
AP-360 "28F008SA Software Drivers"	292095
iMC001FLKA 1-Mbyte Flash Memory Card	290399
iMC002FLKA 2-Mbyte Flash Memory Card	290412
iMC004FLKA 4-Mbyte Flash Memory Card	290388

REVISION HISTORY

Number	Description
02	Added 150 ns TUPLE, Deleted 250 ns TUPLE Corrected Global Power Register Address to 4002H Corrected Write Protection Register Address to 4104H Corrected Ready-Busy Mode Register Address to 4140H I_{CC} Standby Byte Wide Mode MAX/TYP Increased Added Power-On Timing Spec Added First Access after Reset Spec Changed Advanced Information to Preliminary